Design of bendable high-frequency circuits based on short-channel InGaZnO TFTs

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I. Summary And Motivation

A unique requirement of flexible electronic systems is the need to simultaneously optimize their electrical and mechanical performance. Amorphous InGaZnO thin-film transistors (TFTs) fabricated on free-standing large-area plastic substrates address this issue by providing a carrier mobility >10 cm^2/Vs, and bendability down to radii as small as 25 µm. At the same time, limitations such as a constrained minimum lateral feature size, the lack of appropriate p-type materials, or the influence of strain have to be considered when designing circuits. Here, models describing the scaling and bending behavior of flexible InGaZnO TFTs, together with the design of strain insensitive circuits operating at megahertz frequencies are presented.

II. Introduction

Flexible, unobtrusive and cheap sensor devices fabricated on imperceptible substrates and combined with everyday objects, are the next major milestone for smart assistance systems and healthcare products [1-3]. Besides sensors, flexible conditioning circuits and data transceivers are needed to enable such applications. In this context, amorphous InGaZnO (IGZO) TFTs have been identified as a promising technology to fabricate flexible electronics [4]. This is due to the good electrical properties of IGZO [5], and its ability to be deposited on a variety of deformable but temperature sensitive substrates [6, 7]. At the same time, the use of flexible substrates can lead to strain induced performance variations and imposes limitations on the fabrication process, which limits the circuit complexity. All this has to be considered when designing flexible circuits.

III. Results and Methodology

The TFTs shown here are fabricated on free-standing 50 µm thick polyimide using UV lithography. Fig. 1a shows the device structure. The substrate is first encapsulated with 50 nm SiN [PECVD]. A 35 nm thick Cr gate is then e-beam evaporated and wet etched. The gate is insulated by 25 nm Al_2O_3 [ALD] deposited at 150°C, which is the highest temperature used in the fabrication process. Next, 15 nm IGZO are RF sputtered in an Ar atmosphere. The Al_2O_3 and IGZO are independently structured by wet etching. The source and drain contacts (as well as interconnection lines for circuits) are made from 10 nm Ti, and 75 nm Au, e-beam evaporated and structured by lift-off. Finally, the devices are passivated by an additional 25 nm thick Al_2O_3 layer. Fig. 1b shows a fully processed substrate.

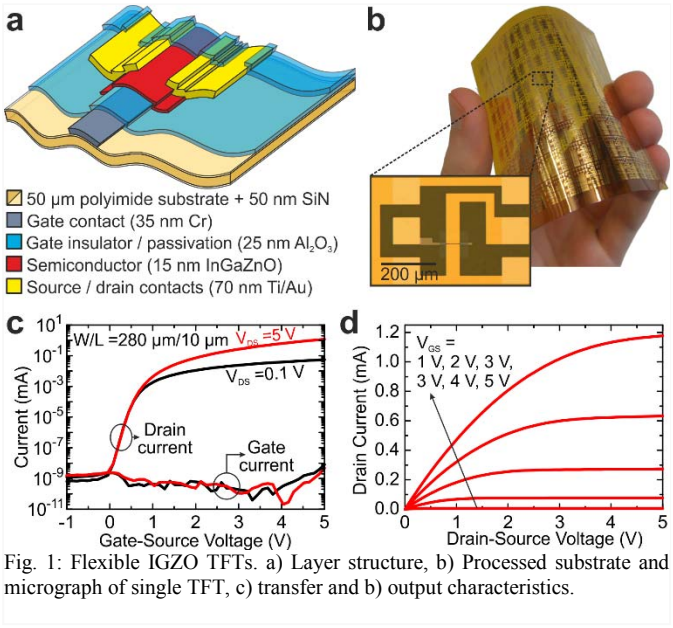

Fig. 1: Flexible IGZO TFTs. a) Layer structure, b) Processed substrate and micrograph of single TFT, c) transfer and b) output characteristics.

Representative transfer and output characteristics of a single TFT are plotted in Figs. 1c and 1d. The shown TFT exhibits a threshold voltage (V_{TH}) of 1 V, a field effect mobility (μ_{FE}) of 15.5 cm^2/Vs, an on/off current ratio >10^8, a subthreshold swing of 110 mV/dec., and a maximum transconductance of 570 µS.

A. Mechanical strain

Minimizing the impact of mechanical deformation is of primary importance when dealing with flexible circuits. Figs. 2a and 2b show a bending test and the parameter shifts caused by strain parallel to the channel. Tensile strain increases μ_{FE} and decreases V_{TH}, while compressive strain has the opposite effect [8]. These shifts are reversible, but excessive stain beyond ≈0.7% tensile or ≈2.2% compressive (bending radii of 3.5 mm and 1.1 mm, respectively [9]) cause cracks and permanently destroys the devices. Although the tolerable tensile strain and minimum bending radius can be improved to 1.7% and 25 µm by using encapsulation layers [10], thin substrates [11], or ductile materials [12], circuits have to consider bending effects. Therefore a SPICE level 61 transistor model was modified to simulate the influence of strain [13].

In particular for digital circuits where the output voltage depends on the transconductance ratio between multiple TFTs

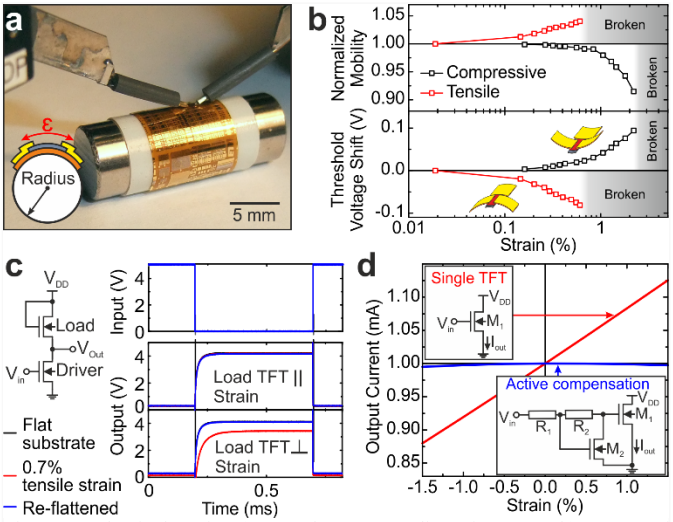

Fig. 2: Mechanical strain. a) TFTs bent to a radius of 3.5 mm. b) Impact of tensile and compressive strain on TFT performance. c) Input and output voltages of flexible IGZO inverters when load and diver TFTs are aligned parallel and perpendicular. d) Simulated output current of a TFT with and without strain compensation circuit under tensile and compressive strain.

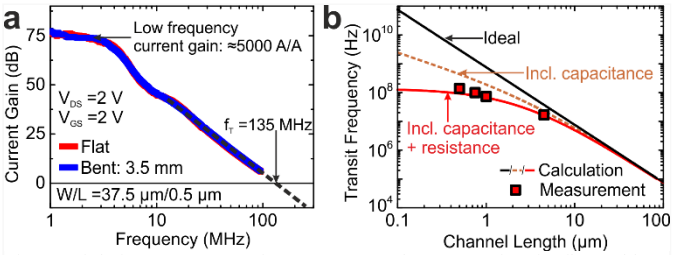

Fig. 3: High frequency operation. a) Measured current gain of a flat and bent IGZO TFT. b) Calculated scaling behaviour of the transit frequency for ideal and realistic scaling models, and corresponding measurements.

parallel alignment of all TFTs is essential. This ensures that bending alters the performance of all TFTs in the same way, and is illustrated in Fig. 2c [14]. Contrarily, if the output current of a single TFT has to be independent of strain, an active feedback, adjusting the gate voltage can be used [13]. Fig. 2d shows that, such circuits can nearly completely eliminate the strain dependency. However, this circuitry (inset of Fig. 2d) requires additional chip area for less strain sensitive passive components, and increases the power consumption by 4.7%.

B. *Scaling and AC performance*

The transit frequency (f_T) can be used to quantify the speed of a TFT, through the unity current gain frequency as shown in Fig. 3a. Traditionally, f_T is inversely proportional to the square of the channel length (L_{CH}). However, for flexible circuits the device fabrication on free-standing plastic foils causes expansion and contraction of the substrate. A typical 7×7 cm^2 polyimide substrate deforms by ≈25 µm [15] Consequently, this limits the minimum feature size, and requires alignment tolerances which in turn influence the parasitic capacitance and contact resistance in the TFTs. It was found that this behaviour can be modelled using the following equation [16]:

$$f_T = \left[\frac{g_{m,0}}{2\pi \cdot C_{ox} \cdot L_{CH}^2}\right] \times \left[\frac{L_{CH}}{L_{CH}+2\cdot L_{OV}}\right] \times \left[\frac{L_{CH}}{L_{CH}+g_{m,0}\cdot \Re_C\{L_{OV}\}}\right] \quad (1)$$

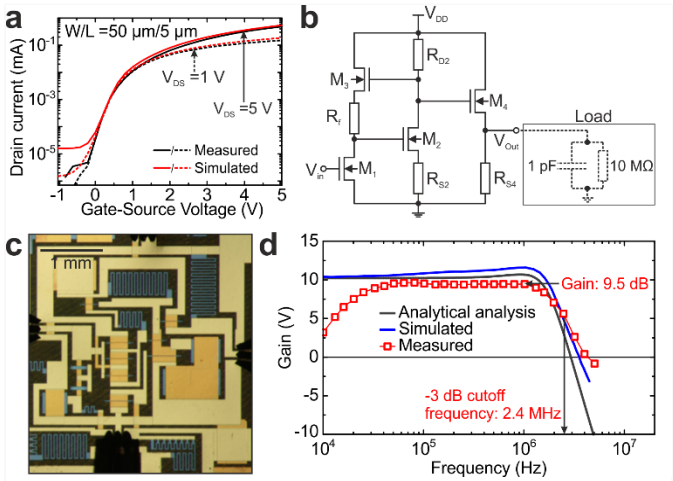

Fig. 4: Circuit simulation. a) Measured and simulated transfer characteristic. b) Simplified circuit schematic and c) micrograph of a Cherry-Hooper amplifier fully integrated on plastic, d) Corresponding simulated and measured voltage gain. The voltage gain drops for frequencies below 50 kHz because of a low-pass filter in the measurement setup which is not part of the simulation.

Eq. 1 depends on the normalized ideal transconductance of an IGZO TFT g_{m0}, the gate insulator capacitance C_{ox}, the gate to source/drain overlap L_{OV}, and the L_{OV} dependent contact resistance $\Re_C\{L_{OV}\}$. The first term of (1) represents the ideal f_T. The following two terms are penalty factors for the overlap capacitance and contact resistance. Fig. 3b validates this model and illustrates the saturating scaling behaviour of these TFTs. However, 0.5 µm short TFTs demonstrated an f_T of 135 MHz, and a maximum frequency of oscillation >300 MHz [17].

C. *Simulation and circuit design*

Finally, the design process of flexible IGZO circuits itself has to consider the fact that no p-type oxide semiconductor with performance comparable to IGZO is available. This requires the design of circuits with NMOS [18], or pseudo-CMOS [19] topology. Furthermore, models to simulate analog IGZO TFT based circuits are required. Fig. 4a shows the measured drain current versus gate-source voltage and compares it to the current predicted by a bespoke compact thin-film transistor model [20]. This model builds on the RPI-aTFT model (Rensselaer Polytechnic Institute model for amorphous silicon TFT) [21], which was improved over the standard model by adding equations and parameters to enhance the prediction accuracy for IGZO TFTs. It also uses binning to enable the modelling of the non-monotonic channel length dependent threshold voltage of the a-IGZO TFTs. The model matches the measurement for a wide range of V_{GS} and V_{DS} values, especially all regions relevant for typical RF circuit design.

To illustrate the capabilities of the presented devices and models, the simplified circuit schematic and a die micrograph of a Cherry-Hooper amplifier with source follower feedback (M_3) and source follower output buffer (M_4, R_{S4}) are shown in Figs. 4b and 4c. This topology was chosen because it results in a high gain-bandwidth product (GBWP). The amplifier provides a voltage gain of 9.5 dB and a GBWP of 7.2 MHz from a 6 V supply, while consuming 6 mW of power. Fig. 4d compares the measured and simulated voltage gain, showing a good agreement between simulation and measurement.

REFERENCES

[1] A. Nathan, A. Ahnood, M. T. Cole, S. Lee, Y. Suzuki, P. Hiralal*, et al.*, "Flexible Electronics: The Next Ubiquitous Platform," *Proceedings of the Ieee,* vol. 100, pp. 1486-1517, May 2012.

[2] K. Myny, "The development of flexible integrated circuits based on thin-film transistors," *Nature Electronics,* vol. 1, p. 30, 2018.

[3] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara*, et al.*, "An ultra-lightweight design for imperceptible plastic electronics," *Nature,* vol. 499, pp. 458-463, Jul 25 2013.

[4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol. 432, pp. 488-492, Nov 25 2004.

[5] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella*, et al.*, "Metal oxide semiconductor thin-film transistors for flexible electronics," *Applied Physics Reviews,* vol. 3, p. 021303, 2016.

[6] R. Martins, I. Ferreira, and E. Fortunato, "Electronics with and on paper," *Physica Status Solidi-Rapid Research Letters,* vol. 5, pp. 332-335, Sep 2011.

[7] G. Cantarella, V. Costanza, A. Ferrero, R. Hopf, C. Vogt, M. Varga*, et al.*, "Design of Engineered Elastomeric Substrate for Stretchable Active Devices and Sensors," *Advanced Functional Materials,* vol. 28, p. 1705132, 2018.

[8] N. Münzenrieder, K. H. Cherenack, and G. Tröster, "The Effects of Mechanical Bending and Illumination on the Performance of Flexible IGZO TFTs," *IEEE Transactions on Electron Devices,* vol. 58, pp. 2041-2048, Jul 2011.

[9] H. Gleskova, S. Wagner, and Z. Suo, "a-Si : H thin film transistors after very high strain," *Journal of Non-Crystalline Solids,* vol. 266, pp. 1320-1324, May 2000.

[10] T. Kinkeldei, N. Münzenrieder, C. Zysset, K. Cherenack, and G. Tröster, "Encapsulation for Flexible Electronic Devices," *Ieee Electron Device Letters,* vol. 32, pp. 1743-1745, Dec 2011.

[11] G. A. Salvatore, N. Münzenrieder, T. Kinkeldei, L. Petti, C. Zysset, I. Strebel*, et al.*, "Wafer-scale design of lightweight and transparent electronics that wraps around hairs," *Nat Commun,* vol. 5, p. 2982, 2014.

[12] N. Münzenrieder, L. Petti, C. Zysset, D. Görk, L. Büthe, G. A. Salvatore*, et al.*, "Investigation of gate material ductility enables flexible a-IGZO TFTs bendable to a radius of 1.7 mm," *Solid-State Device Research Conference (ESSDERC), 2013 Proceedings of the European,* pp. 362-365, 16-20 Sept. 2013 2013.

[13] W. M. H. bin Wan Zaidi, J. Costa, A. Pouryazdan, W. F. H. Abdullah, and N. Münzenrieder, "Flexible IGZO TFT SPICE model and design of active strain-compensation circuits for bendable active matrix arrays," *IEEE Electron Device Letters,* vol. 39, pp. 1314-1317, 2018.

[14] N. Münzenrieder, C. Zysset, T. Kinkeldei, and G. Tröster, "Design Rules for IGZO Logic Gates on Plastic Foil Enabling Operation at Bending Radii of 3.5 mm," *Ieee Transactions on Electron Devices,* vol. 59, pp. 2153-2159, Aug 2012.

[15] N. Münzenrieder, L. Petti, C. Zysset, T. Kinkeldei, G. A. Salvatore, and G. Tröster, "Flexible Self-Aligned Amorphous InGaZnO Thin-Film Transistors With Submicrometer Channel Length and a Transit Frequency of 135 MHz," *Ieee Transactions on Electron Devices,* vol. 60, pp. 2815-2820, Sep 2013.

[16] N. Münzenrieder, G. A. Salvatore, L. Petti, C. Zysset, L. Büthe, C. Vogt*, et al.*, "Contact resistance and overlapping capacitance in flexible sub-micron long oxide thin-film transistors for above 100 MHz operation," *Applied Physics Letters,* vol. 105, p. 263504, 2014.

[17] N. Münzenrieder, K. Ishida, T. Meister, G. Cantarella, L. Petti, C. Carta*, et al.*, "Flexible InGaZnO TFTs with fmax above 300 MHz," *IEEE Electron Device Letters,* vol. 39, pp. 1310 - 1313, 2018.

[18] R. Shabanpour, T. Meister, K. Ishida, B. Kheradmand-Boroujeni, C. Carta, F. Ellinger*, et al.*, "Design and analysis of high-gain amplifiers in flexible self-aligned a-IGZO thin-film transistor technology," *Analog Integrated Circuits and Signal Processing,* vol. 87, pp. 213-222, May 2016.

[19] K. Ishida, R. Shabanpour, B. K. Boroujeni, T. Meister, C. Carta, F. Ellinger*, et al.*, "22.5 dB Open-Loop Gain, 31 kHz GBW Pseudo-CMOS Based Operational Amplifier with a-IGZO TFTs on a Flexible Film," *2014 Ieee Asian Solid-State Circuits Conference (a-Sscc),* pp. 313-316, 2014.

[20] R. Shabanpour, T. Meister, K. Ishida, B. Boroujeni, C. Carta, F. Ellinger*, et al.*, "A Transistor Model for a-IGZO TFT Circuit Design Built Upon the RPI-aTFT Model," *IEEE NEWCAS,* pp. 129-132, 2017.

[21] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, "SPICE models for amorphous silicon and polysilicon thin film transistors," *Journal of the Electrochemical Society,* vol. 144, pp. 2833-2839, 1997.