Metal oxide semiconductor thin-film transistors for flexible electronics

Article (Accepted Version)


This version is available from Sussex Research Online: http://sro.sussex.ac.uk/id/eprint/61869/

This document is made available in accordance with publisher policies and may differ from the published version or from the version of record. If you wish to cite this item you are advised to consult the publisher's version. Please see the URL above for details on accessing the published version.

Copyright and reuse:
Sussex Research Online is a digital repository of the research output of the University.

Copyright and all moral rights to the version of the paper presented here belong to the individual author(s) and/or other copyright owners. To the extent reasonable and practicable, the material made available in SRO has been checked for eligibility before being made available.

Copies of full text items generally can be reproduced, displayed or performed and given to third parties in any format or medium for personal research or study, educational, or not-for-profit purposes without prior permission or charge, provided that the authors, title and full bibliographic details are credited, a hyperlink and/or URL is given for the original metadata page and the content is not changed in any way.
The field of flexible electronics has rapidly expanded over the last decades, pioneering novel applications, such as wearable and textile integrated devices, seamless and embedded patch-like systems, soft electronic skins, as well as imperceptible and transient implants. The possibility to revolutionize our daily life with such disruptive appliances has fueled the quest for electronic devices which yield good electrical and mechanical performance, and are at the same time light-weight, transparent, conformable, stretchable, and even biodegradable. Flexible metal oxide semiconductor thin-film transistors (TFTs) can fulfill all these requirements, and are therefore considered the most promising technology for leading tomorrow’s electronics. This review reflects the establishment of flexible metal oxide semiconductor TFTs, from the development of single devices, large-area circuits, up to entire integrated systems. First, an introduction on metal oxide semiconductor TFTs is given, where the history of the field is revisited, the TFT configurations and operating principles are presented, and the main issues and technological challenges faced in the area are analyzed. Then, the recent advances achieved for flexible n-type metal oxide semiconductor TFTs manufactured by physical vapor deposition methods as well as solution-processing techniques are summarized. In particular, the ability of flexible metal oxide semiconductor TFTs to combine low temperature fabrication, high carrier mobility, large frequency operation, extreme mechanical bendability, together with transparency, conformability, stretchability, as well as water dissolubility is shown. Afterward, a detailed analysis of the most promising metal oxide semiconducting materials developed to realize state-of-the-art flexible p-type TFTs is given. Next, the recent progresses obtained for flexible metal oxide semiconductor-based electronic circuits, realized with both unipolar and complementary technology are reported. In particular, the realization of large-area digital circuitry like flexible near field communication tags, as well as analog integrated circuits like bendable operational amplifiers is presented. The last topic of this review is devoted to emerging flexible electronic systems such as foldable displays, integrated sensoric systems, power transmission elements, as well as large-area data storage and transmission systems. Finally, the conclusions are drawn and an outlook over the field is provided.

I. INTRODUCTION

Electronics today is facing a disruptive evolution, advancing from heavy, bulky and rigid devices to light-weight, soft and flexible appliances. Emerging new applications like smart labels\(^1\) and intelligent packaging,\(^2\) wearable\(^1\textsuperscript{--}^4\) and textile integrated systems,\(^5\textsuperscript{--}^7\) seamless and embedded patch-like electronics,\(^8\textsuperscript{,}^9\) epidermal devices,\(^10\textsuperscript{--}^16\) artificial skins for robots,\(^17\textsuperscript{--}^19\) imperceptible\(^20\textsuperscript{,}^21\) biomimetic\(^22\) and transient\(^23\textsuperscript{--}^25\) medical implants, as well as advanced surgical tools\(^13\textsuperscript{,}15\textsuperscript{,}16\textsuperscript{,}26\textsuperscript{,}27\) promise to revolutionize our daily life. To enable all these applications, electronic devices have to become flexible, light-weight, transparent, conformable, stretchable and even biocompatible and biodegradable. Flexible thin-film transistors (TFTs) are able to fulfill all these requirements, and are thus becoming increasingly important to realize next-generation electronic
device platforms. Among state-of-the-art flexible TFT technologies, metal oxide semiconductors are especially suitable, owing to their high optical transparency,\textsuperscript{28} good electrical performance [electron carrier mobility \(\geq 10 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) even if processed at room-temperature (RT)],\textsuperscript{28} as well as excellent mechanical properties (large bendability down to 25\(\mu\)m radii\textsuperscript{22} and good insensitivity to strain\textsuperscript{29}). Table I provides a summary and a comparison of the most important device properties for the established flexible TFT technologies: amorphous silicon (a-Si),\textsuperscript{14,32} organic semiconductors,\textsuperscript{14,32} low temperature poly-crystalline silicon (LTPS),\textsuperscript{33,34} and metal oxide semiconductors. As evident from Table I, metal oxide semiconducting technology presents several advantages over a-Si and organic materials, such as low cost, low process complexity and temperature, large-area scalability, but at the same time yields a larger carrier mobility.\textsuperscript{35} Compared to LTPS, metal oxide semiconductors present slightly lower carrier mobility, but also larger area scalability, smaller manufacturing cost, as well as process complexity and temperature.\textsuperscript{35} Furthermore, metal oxide semiconductor TFTs show a larger resistance to mechanical strain if compared to LTPS devices.\textsuperscript{29} This is why metal oxide semiconductors are considered the most prominent candidate for next-generation flexible high-resolution active matrix organic light emitting display (AMOLED) backplanes,\textsuperscript{38–41} as well as the most suitable technology to fuel the realization of tomorrow’s ubiquitous electronics. Main aim of this review is to report the recent advances obtained in the field of flexible metal oxide semiconductor TFTs: from single devices (sections II and III), large-area circuits (section IV), up to entire integrated systems (section V). Before reviewing the state-of-the-art of flexible metal oxide semiconductor technology in the next sections, in this section an introduction on the topic is given. First, a historical overview on TFTs based on metal oxide semiconductors is presented in I A. Next, in 1B the operating principle of TFTs, together with the available device configurations are reported. Subsequently, in 1C the main issues and technological challenges faced in the field are analyzed. Finally, at the end of 1C the structure of the review is outlined in detail.

A. Historical perspective

TFTs find their origin back in the 1930 when the field-effect transistor (FET) concept was patented by Lilienfeld.\textsuperscript{42–44} In these reports, Lilienfeld described the concept of a device in which the current flow is controlled by the application of a transversal electric field. Even if TFTs and FETs share the same operating principle, the first TFTs were realized only in 1962 by Weimer at RCA laboratory.\textsuperscript{45} In his work, Weimer used a vacuum technique (evaporation) and high-precision shadow masking to deposit and structure gold (Au) source/drain (S/D) electrodes, a micro-crystalline cadmium sulfide (CdS) n-type (electron conducting) semiconductor, a silicon monoxide gate dielectric and an Au gate contact on an insulating glass substrate (Fig. 1). Interestingly, Weimer already showed a preliminary evaluation of thin-film circuits, such as flip-flops, AND and NOR gates. His proceeding of IRE ”The TFT – a new Thin-Film Transistor” draw worldwide attention,\textsuperscript{45} opening the way to a new field of study. Few years later in 1964, the first TFT with a metal oxide semiconductor was demonstrated by Klasens and Koelmans.\textsuperscript{46} The device was manufactured by photolithographic techniques and comprised aluminum (Al) electrodes, anodized aluminum oxide (Al\(_2\)O\(_3\)) gate dielectric, evaporated n-type tin oxide (SnO\(_2\)) semiconductor, and source/drain contacts on a glass substrate. For the first time, the transparency of substrate, semiconductor, and gate dielectric allowed realizing a self-aligned (SA) lithographic lift-off process, where the source/drain contacts were defined by exposing the photoresist to ultraviolet (UV) light penetrating from the back of the substrate. In this way, the opaque Al gate electrode could act as a shielding layer for the UV light.\textsuperscript{46} Subsequently, TFTs with single crystal lithium-doped zinc oxide (ZnO:Li) hydrothermically grown from solution,\textsuperscript{47} as well as SnO\(_2\) deposited from vapor phase reaction were presented.\textsuperscript{48} Nevertheless, none of these two devices outperformed the results shown by Klasens and Koelmans. After a few decades of silence, in 1996 metal oxide semiconductors gained new attention as active layers in ferroelectric memory TFTs.\textsuperscript{49,50} The pioneering work of Prins et al. demonstrated the first fully transparent and metal oxide-based TFT with antimony-doped SnO\(_2\) (SnO\(_2\):Sb) semiconductor grown by pulsed layer deposition (PLD) (Fig. 2).\textsuperscript{49} At the same time, Seager et al. showed the first indium oxide (In\(_2\)O\(_3\)) non-volatile memory TFT with ferroelectric gate dielectric.\textsuperscript{50} Following the success of these works, from 2003 metal oxide semiconductors gained an increasingly interest. The majority of the attention was initially directed to zinc oxide (ZnO)
months later, Carcia et al. reported fully transparent ZnO TFTs yielding a mobility of 2 cm² V⁻¹ s⁻¹. In this context, Hoffman, Norris, and Wager reported on a-Si, commonly employed in TFT display backplanes. The suitability of this technology as a replacement for TFTs, 1996 (reproduced from Prins et al. with permissions from AIP).⁵⁹

Additionally, also TFTs with other binary metal oxide semiconductors like In₂O₃ and SnO₂ were reported, yielding also good performance.⁶¹,⁶² Main breakthrough in the field was achieved in 2003 by Nomura et al. who demonstrated a multicomponent indium gallium zinc oxide (IGZO) single-crystalline active layer epitaxially grown at 1400 °C on an yttria-stabilized zirconium (YSZ) substrate.⁶³ The resulting TFT presented a mobility of 80 cm² V⁻¹ s⁻¹ and a current on/off ratio of 10⁶, demonstrating that high-performance TFTs can be realized with metal oxide semiconductors.

Continuing their work, in 2004 Nomura et al. reported transparent TFTs with amorphous IGZO layers grown at room-temperature by PLD on flexible polyethylene terephthalate (PET) foils (Fig. 3).²⁸ The results were impressive (especially considering the low temperature process): an electron carrier mobility of 9 cm² V⁻¹ s⁻¹ and a current on/off ratio of 10⁷. Furthermore, first mechanical bending tests of the devices at 30 mm radius were demonstrated. Nomura’s report paved the way to an impressive number of publications on metal oxide semiconductor TFTs. In the following years, several multicomponent metal oxide semiconductors, ranging from zinc tin oxide (ZTO),⁶⁴,⁶⁵ indium zinc oxide (IZO),⁶⁶ to IGZO (the most common)⁶⁷-⁶⁹ were investigated. From 2005, also the first reports on p-type SnO₂ TFTs,⁷⁰ followed by other works on p-type tin monoxide (SnO)₇¹,⁷² cuprous oxide (Cu₂O),⁷³,⁷⁴ and nickel oxide (NiO)⁷⁵ devices all presenting low mobility and high process temperatures. Remarkably, in 2007 Ju et al. showed the first flexible and solution-processed metal oxide semiconductor TFTs,⁷⁶ From 2008, tremendous advances were made in the field of flexible devices, from IGZO TFTs on cellulose fiber-based paper,⁷⁷ stretchable and transparent ZnO TFTs,⁷⁸,⁷⁹ complementary inverters (NOT gates) based on n-type IGZO and p-type SnO TFTs with and on paper,⁸⁰ ultraflexible and transparent IGZO TFTs,⁸¹

<table>
<thead>
<tr>
<th>Metal oxide semiconductors</th>
<th>Microstructure</th>
<th>Mobility (cm² V⁻¹ s⁻¹)</th>
<th>Manufacturing cost</th>
<th>Process complexity</th>
<th>Process temperature (°C)</th>
<th>Large-area scalability</th>
<th>Device type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amorphous silicon</td>
<td>Amorphous</td>
<td>1</td>
<td>Low</td>
<td>Low</td>
<td>RT to 250</td>
<td>High</td>
<td>N-type</td>
</tr>
<tr>
<td>Low temperature poly-crystalline silicon</td>
<td>Poly-crystalline</td>
<td>50-100</td>
<td>High</td>
<td>High</td>
<td>350-500</td>
<td>Low</td>
<td>N- and p-type</td>
</tr>
</tbody>
</table>

Table I. Comparison between metal oxide semiconductors and other available flexible TFT technologies.⁸,³⁴-³⁷

Figure 2. a) Device cross-section and b) photograph of the first fully transparent metal oxide-based TFT reported in 1996 (reproduced from Prins et al. with permissions from AIP).⁵⁹

Figure 3. First flexible TFT with indium gallium zinc oxide (IGZO) active layer reported in 2004: a) cross-section and b) photograph of TFT bent to 30 mm tensile radius (adapted from Nomura et al. with permissions from Nature Publishing Group).²⁸
three-dimensionally (3D) conformable IGZO TFTs and circuits,\textsuperscript{81} water soluble IGZO TFTs,\textsuperscript{82} to mechanically active biomimetic IGZO TFTs.\textsuperscript{22} Nowadays, state-of-the-art flexible IGZO TFTs yield excellent electrical performance with reported carrier mobility values up to 84 cm\(^2\) V\(^{-1}\) s\(^{-1}\),\textsuperscript{83} and current on/off ratio > 10\(^{10}\),\textsuperscript{84} depending on the semiconductor composition and device configuration.

B. TFT configuration and operation

In this subsection, the most common TFT configurations will be presented, followed by a short explanation of the basic TFT operating principle.

**TFT configuration:** TFTs are three terminal field-effect devices, whose working principle is similar to those of metal oxide semiconductor field-effect transistors (MOSFET) used in conventional Silicon (Si) electronics.\textsuperscript{85} However, in MOSFET technology the substrate is a single crystal Si wafer (representing also the active layer) and device functionality is added through a large variety of complex, high-temperature (> 1000\(^\circ\)C) and expensive processes (e.g. diffusion/implantation of dopants, lithography, etching).\textsuperscript{86} On the other hand, TFTs are fabricated typically on insulating substrates (glass, plastic), on which all the device layers are grown at lower temperature (< 650\(^\circ\)C) by vacuum- or solution-processing deposition techniques. Given the different manufacturing process, the active layers of TFTs are typically poly-crystalline or amorphous materials, which are both characterized by a reduced charge carrier transport (if compared to single-crystal Si).\textsuperscript{35,87} Like in MOSFETs, TFT functionality is achieved through the following components: a dielectric layer inserted between the semiconductor and a trasversal gate contact, together with two source/drain electrodes directly in contact with the semiconductor. Current modulation between source/drain is achieved through the semiconducting layer by the capacitive injection of carriers close to the dielectric/semiconductor interface (the so-called field-effect).\textsuperscript{85} Even if both MOSFETs and TFTs rely on the field-effect to modulate the conductance of the active layer, in TFTs this is achieved by an accumulation layer (and not an inversion region like in MOSFETs). TFTs can be fabricated using a wide range of device configurations. Most peculiar planar TFT structures are: bottom-gate (BG) (Fig. 4a-b) and top-gate (TG) (Fig. 4c-d) architectures, depending whether the gate electrode is deposited before or after the active layer. BG and TG devices can be either staggered or coplanar, depending if the source/drain contacts are on the opposite or on the same side of the semiconductor/dielectric interface.\textsuperscript{85} BG structures, especially staggered (Fig. 4a) have been widely used for a-Si TFTs, as well as in most display prototypes due to easier processing and enhanced performance.\textsuperscript{35,88} Nevertheless, BG structures require an additional layer (passivation) that protects the back channel from air exposure and therefore hinders undesired instability effects.\textsuperscript{35,88} TG structures, especially coplanar (Fig. 4d) have been mainly used for LTPS technology. With such a configuration indeed, the semiconductor can be deposited and crystallized at high temperatures without any damage to other materials/interfaces that are realized in successive steps.\textsuperscript{33} In TG TFTs, the gate dielectric can also act as a passivation layer, reducing thus the number of patterning steps.\textsuperscript{28,88} To improve the static (DC) performance, double-gate (DG) TFT structures (Fig. 4e) can be employed.\textsuperscript{89,90} In DG TFTs, an additional gate is utilized to effectively control a larger portion of the semiconductor channel. Recently, the quest for small device footprint and nanoscaled channel lengths (L) has led to the development of alternatives to planar geometries, such as vertical TFTs (VTFTs) (Fig. 4f) or quasi-vertical TFTs (QVTFTs), where the channel is not anymore defined by a photolithographic patterning step, but rather by the thickness of a device layer.\textsuperscript{91,92} In the most common VTFT structures, the channel is formed on a multi-layer stack of source-dielectric-drain (Fig. 4e) \textsuperscript{91–93} Nevertheless, alternative VTFT configurations with the channel defined by the gate or the semiconductor thickness have also been proposed and realized.\textsuperscript{94–96}

**TFT operation:** The most important DC performance parameters are extracted from the current-voltage (I-V) characteristics in compliance with the gradual channel approximation.\textsuperscript{97} As shown in the transfer
Figure 5. Typical current-voltage characteristics of an n-type metal oxide semiconductor TFT (channel length L = 30 µm): width (W) normalized transfer (a) and output (b) curves.

$I_D$-$V_{GS}$ (Fig. 5a) and output $I_D$-$V_{DS}$ (Fig. 5b) curves, there are two main operating regimes: linear and saturation. For small values of the drain-source voltage $V_{DS}$ ($V_{DS} \ll V_{GS} - V_{TH}$, where $V_{GS}$ is the gate-source voltage and $V_{TH}$ the threshold voltage), the device operates in linear regime and the drain current $I_D$ is approximated by the following formula given by the simplified Shichman-Hodges FET model:58

$$I_{D,lin} = \frac{W \cdot \mu \cdot C_{ox}}{L} \cdot (V_{GS} - V_{TH}) \cdot V_{DS}, \quad (I.1)$$

where $W$ is the channel width, $\mu$ is the channel mobility and $C_{ox}$ is the specific capacitance of the gate dielectric per unit area. When $V_{DS} \geq V_{GS} - V_{TH}$, the device operates in saturation regime and $I_D$ equals:

$$I_{D,sat} = \frac{W \cdot \mu \cdot C_{ox}}{2L} \cdot (V_{GS} - V_{TH})^2, \quad (I.2)$$

Equation I.1 and I.2 can be used to extract the TFT DC parameters: carrier mobility, threshold voltage, current on/off ratio, sub-threshold swing, and contact resistance.97

**Carrier mobility:** This parameter describes the efficiency of charge carrier transport in a material, which affects directly the maximum drain current and the operating frequency (the so-called transit frequency $f_T$) of a device.99 In a material $\mu$ depends on several scattering mechanisms (e.g. lattice vibrations, impurities, grain boundaries).99,100 The most common way to characterize the intrinsic mobility of a bulk material is to extract the Hall mobility ($\mu_H$) from the Hall effect.100 The mobility in a TFT is typically different from the intrinsic mobility of its semiconductor, since charge transfer is now limited to a narrow region close to the gate dielectric/semiconductor interface and further sources of scattering (e.g. Coulomb scattering from dielectric charges and interface states, surface roughness scattering) need to be considered.100 According to Schroder,100 several TFT mobilities can be extracted: the effective mobility $\mu_{eff}$, the field-effect mobility $\mu_{FE}$, and the saturation mobility $\mu_{sat}$. Most common mobilities are $\mu_{FE}$ (also known as linear mobility $\mu_{lin}$):

$$\mu_{FE} = \mu_{lin} = \frac{L}{W \cdot C_{ox} \cdot V_{DS}} \cdot \frac{dI_D}{dV_{GS}}, \quad (I.3)$$

and $\mu_{sat}$:

$$\mu_{sat} = \frac{2 \cdot L}{W \cdot C_{ox}} \cdot \frac{d^2I_D}{dV_{GS}^2} = \frac{2 \cdot L}{W \cdot C_{ox}} \cdot \left(\frac{d\sqrt{I_D}}{dV_{GS}}\right)^2. \quad (I.4)$$

**Threshold voltage:** The threshold voltage $V_{TH}$ corresponds to the $V_{GS}$ at which a conductive channel is formed at the dielectric/semiconductor interface.97 In n-type TFTs, if $V_{TH}$ is positive/negative the devices are designated to operate in enhancement/depletion mode.51 There are several methods used to extract $V_{TH}$.101 If not explicitly specified, the most employed methodology is represented by the linear extrapolation of the $I_D$-$V_{GS}$ plot (linear regime) or $I_{D}^{1/2}$-$V_{GS}$ plot (saturation regime).101

**Current on/off ratio:** The current on/off ratio $I_{ON}/I_{OFF}$ is extracted from the transfer curve (Fig. 5a) dividing the maximum with the minimum $I_D$ (typically in saturation regime).97 A value of $10^8$ or higher is desirable for digital circuits.102 Nevertheless, smaller $I_{ON}/I_{OFF}$ can also result in successful switching operation.103 For analog circuits an $I_{ON}/I_{OFF} > 10^4$ is typically sufficient.80

**Sub-threshold swing:** Another important parameter is the sub-threshold swing (SS), which is a measure of how efficiently the transistor can turn on and off.
SS is directly related to the quality of the interface dielectric/semiconductor. The sub-threshold swing is defined as the inverse of the maximum slope of the $I_D$-$V_{GS}$ plot and indicates the $V_{GS}$ needed to increase the drain current by one decade:

$$SS = \left(\frac{dV_{GS}}{d\log_{10}(I_D)}\right)_{max}. \quad (I.5)$$

A low sub-threshold swing <100 mV/dec (together with a threshold voltage close to 0 V) is desirable to reduce the power consumption and the operating voltages in circuit applications. 

**Contact resistance:** Beside the above mentioned parameters, a less cited (but still important) parameter is given by the contact resistance ($R_C$) between the source/drain electrodes and the semiconductor. Controlling the contact resistance is especially important in short-channel devices ($L < 5 \mu m$), since a high $R_C$ value can lead to the degradation of both the device performance and the overlap capacitance. 

The overlap capacitance ($C_{OV}$) between the gate and source/drain electrodes is an important parameter, since it reduces the TFT’s $I_T$. In a TFT, the contact resistance ($R_C$) can be estimated from the total TFT resistance ($R_T$):

$$R_T = r_{CH} \cdot L + R_C, \quad (I.6)$$

where $r_{CH}$ is the channel resistance per unit channel length. By fitting the experimental values of the $R_T$-$L$ plot for different $V_{GS}$ with a linear curve, the total $R_C$ can be estimated. Alternatively, the contact resistance can be also extracted from the ratio of two linear $I_D$-$V_{GS}$ measurements taken on the same device (at two different $V_{DS}$), as explained by Campbell et al. 

**Overlap capacitance:** Besides the contact resistance, also the overlap capacitance $C_{OV}$ between the gate and the source/drain electrodes is an important parameter, since it reduces the TFT’s $I_T$. In a TFT, $C_{OV}$ can be extracted from the capacitance-voltage (C-V) characteristics (Fig. 6), from which the total gate capacitance $C_G$ can be estimated:

$$C_G = C_{GS} + C_{GD} = C_{ox} \cdot W \cdot (L + L_{OV,TOT}) \quad (I.7)$$

where $C_{GS}$ is the gate-source capacitance, $C_{GD}$ the gate-drain capacitance, and $L_{OV,TOT}$ the total overlap length between gate and source/drain electrodes ($L_{OV,TOT} = L_{OV,S} + L_{OV,D}$). The overlap capacitance $C_{OV} = C_{ox} \cdot W \cdot L_{OV,TOT}$, and can be extracted from the C-V plot (Fig. 6) as the minimum $C_G$ value.

**Transit frequency:** The most important small signal (AC) parameter of a TFT is the transit frequency ($f_T$), which quantifies the speed of the device.

$$f_T = \frac{1}{2 \cdot \pi} \cdot \frac{g_m}{C_G} \propto \frac{\mu \cdot (V_{GS} - V_{TH})}{L \cdot (L + L_{OV,TOT})} \quad (I.8)$$

where $g_m$ is the transconductance ($g_m = \frac{dI_D}{dV_{GS}}$) calculated in the saturation regime. A first approximation of the transit frequency can be calculated from the $g_m$ and $C_G$ values extracted from the $I_D$-$V_{GS}$ and $C_G$-$V_{GS}$ data, respectively. A more precise value of the transit frequency can be extracted from the TFT S-parameters, which can be measured by applying a low voltage RF voltage on top of the $V_{GS}$ bias and subsequently measuring the $I_{DS,sat}$ of the devices. From the device S-parameter measurement, the corresponding small signal current gain $H_21$ can be calculated as a function of the frequency. The $f_T$ is then given by the value where $H_21$ equals 1 (see fig. 13 for a practical example).

### C. Present issues and challenges

From 2003 onwards with the work of Hosono, Wager, Carcin, and Fortunato, metal oxide
semiconductor TFTs have gained an increasingly interest, especially in view of their application in optical display backplanes. At the beginning, the attention has been mainly focused on the realization of metal oxide semiconductor TFT yielding high mobility, as well as good stability under bias and illumination stress. In particular, the influence of semiconductor composition, passivation layer, gate dielectric and source/drain electrodes on the device performance and stability has been extensively investigated, as reported in several reviews.\textsuperscript{35,88,115} The enormous progresses achieved in the last ten years in these areas have directed current research efforts towards new directions and challenges.\textsuperscript{35,88} In particular, the possibility to replace vacuum-processing techniques with higher throughput continuous processes is especially attractive in view of novel large-area and cost-effective applications, such as foldable and printable displays, disposable smart labels and intelligent packaging.\textsuperscript{87,116} To this aim, solution-deposition processes, especially spray pyrolysis (SP) or digitally controlled on-demand deposition methods like ink-jet printing, are attracting an increasing interest.\textsuperscript{87} Another open issue is represented by the development of metal oxide semiconductor TFTs with good p-type conduction. Even if notable advances have been made in this direction, p-type metal oxide semiconductor devices can hardly yield performance levels similar to their n-type counterpart.\textsuperscript{35,87} As explained later in this review, this is due to the specific charge transport characteristics of metal oxide semiconductors.\textsuperscript{115,117} Due to the scarce availability of good p-type devices, the majority of the reported metal oxide semiconductor-based circuits are thus unipolar, employing only n-type TFTs. Even if complex large-area and high TFT count digital and analog electronic circuits have been demonstrated by employing only n-type metal oxide semiconductor TFTs, the development of a complementary technology based on both n- and p-type devices is essential to realize compact and low-power circuits.\textsuperscript{118} To this purpose, research on complementary circuits based on hybrid metal oxide/organic or fully metal oxide semiconducting materials has expanded.\textsuperscript{35}

All of the above mentioned topics apply for both rigid and flexible metal oxide semiconductor TFTs. Nevertheless, in the case of flexible substrates, the solution of the previously listed issues is even more challenging, due to the generally more complicated processing conditions (low temperature fabrication, substrate dimensional instability during TFT fabrication and circuit integration, etc). Furthermore, in the case of flexible TFTs, special care needs to be taken also on the mechanical properties of the devices (e.g. induced strain, maximum strain resistance, influence of strain on the TFT performance, role of mechanical fatigue, etc). Additionally, novel device features like transparency, conformability, stretchability, biocompatibility and biodegradability (with their related challenges) need also to be taken into account. In this review, we will try to tackle all of the above mentioned issues and challenges, focusing only on devices fabricated on flexible substrates. To date and to the best of our knowledge, no report has specifically targeted this topic. We are only aware of a book chapter dealing with flexible solution-processed metal oxide semiconductor TFTs,\textsuperscript{37} as well as two review papers on the mechanical and electronic properties of flexible TFTs (all technologies)\textsuperscript{29} and p-type metal oxide semiconductor materials and devices.\textsuperscript{119} For this reason, this paper will present the recent progresses in the field of flexible TFTs and circuits, based on both n- and p-type metal oxide semiconductors grown by vacuum- and solution-processing techniques. Main aim of this review is to underline the process/material/device/circuit requirements that are specific to flexible substrates compared to rigid ones, and provide at the same time guidelines for the realization of flexible devices with good electrical and mechanical properties, using metal oxide semiconductor technology. The reviews is structured as follows:

- In section II, state-of-the-art flexible n-type metal oxide semiconductor TFTs are presented. First in IIA a short overview of the available metal oxide semiconductors is given. Then in IIB flexible devices based on vacuum-processed metal oxide semiconductors are reviewed. Finally, in IIC flexible TFTs with novel solution-deposited metal oxide semiconductors are reported.

- Section III deals with the recent progresses in the field of flexible p-type metal oxide semiconductor TFTs. As for section II, also in this case first a brief overview on the available materials is given IIIA; then in IIIB flexible devices based on vacuum-processed metal oxide semiconductors are reviewed; finally in IIIC solution-processed flexible TFTs are analyzed.

- Section IV reviews state-of-the-art circuits based on metal oxide semiconductors.IVA provides a basic explanation of the possible configurations, as well as of the basic operating principle of both digital and analog circuits. Then, in IVB flexible unipolar digital and analog electronic circuits based on metal oxide semiconductors are presented. Finally, in IVC flexible complementary metal oxide semiconductor-based circuits are reviewed.

- Section V deals with novel flexible electronic applications based on metal oxide semiconductor TFTs.

- In section VI the conclusions are drawn and an outlook over the field is given.

In order to provide a broad overview of the field, the first subsections of each section (IIA, IIIA, IVA) reference reports on both rigid and flexible substrate. However, the main subsections of this review (IIB, IIC, IIIB, IIIC, IVB, IV C) deal only with flexible TFTs and circuits based on metal oxide semiconducting materials. We
have done an exhaustive literature review on the topic and have tried to include all the relevant works until the submission of this review (March 2016). If there is some work not referenced, we apologize the authors in advance.

II. N-TYPE METAL OXIDE SEMICONDUCTOR TFTs

In this section, flexible n-type metal oxide semiconductor TFTs are presented. In particular, in II A binary and multicomponent metal oxide semiconducting compounds are reported, together with a short explanation on the theory of these materials. Then in II B, a detailed description of the recent progresses obtained for flexible vacuum-processed metal oxide semiconductor TFTs is given, with a special focus on materials, fabrication techniques, electrical performance and bendability. Finally, in II C novel solution-processing methods to realize flexible metal oxide semiconductor TFTs are shown.

A. N-type metal oxide semiconductors

The first reported metal oxide semiconductors were binary compounds, such as SnO$_2$, ZnO, In$_2$O$_3$, and Ga$_2$O$_3$, in either a pure composition or with impurity dopings. These binary materials are characterized by wide band gap $E_g > 3$ eV and large transmission in the visible range (above 80%).$^{115,120}$ The resulting films are n-type semiconducting, yielding a high carrier concentration (N) in the order of $10^{16}$ cm$^{-3}$ - $10^{21}$ cm$^{-3}$, which is attributed to native donors, e.g. oxygen (O$_2$) vacancies and/or metal atoms.$^{115,120}$ Additionally, even if these films present an amorphous phase, they yield large $\mu$FE > 10 cm$^2$ V$^{-1}$ s$^{-1}$.$^{115}$ Due to their unique electronic structure.$^{117}$ Indeed in contrast to covalent semiconductors like Si, metal oxide semiconductors are valence compounds with a strong degree of ionicity within their chemical bonding.$^{87,117}$ In metal oxide semiconductors, charge transfer occurs from the metal orbitals (s) to the oxygen orbitals (2p). The conduction band minimum (CBM) is indeed formed by highly dispersive unoccupied metal orbitals, whereas the valence band maximum (VBM) is constituted by fully occupied and localized oxygen orbitals.$^{87,117}$ Those vacant metal orbitals are spherical (i.e. non directional), and exhibit large spatial spread.$^{115,117}$ As a consequence, electron transport can easily occur through the direct overlap of the metal orbitals in neighboring metal cations.$^{87,115,117}$ This explains why the majority of existing metal oxide semiconductors yields n-type conductivity, and hole transport is intrinsically hindered by a larger effective mass.$^{87}$ By employing binary metal oxide semiconducting materials (SnO$_2$, ZnO, In$_2$O$_3$ and Ga$_2$O$_3$) as active layers in TFTs, large differences in carrier mobility and current on/off ratios can be achieved. For example, In$_2$O$_3$ TFTs can lead to high $\mu$FE up to 100 cm$^2$ V$^{-1}$ s$^{-1}$, but at the same time also large $I_{OFF}$ (due to high N > 10$^{18}$ cm$^{-3}$).$^{35,121}$ Ga$_2$O$_3$ films possess large resistivity (due to low carrier density and large density of empty traps), resulting thereby in poor device performance ($\mu$FE = 0.05 cm$^2$ V$^{-1}$ s$^{-1}$).$^{35,122}$ Similar to In$_2$O$_3$, SnO$_2$ TFTs can reach higher carrier mobility, as well as larger off current.$^{62}$ The best-known and most performing binary metal oxide semiconductor is ZnO, which can lead to high $\mu$FE and $I_{ON}/I_{OFF}$. However, most binary metal oxide semiconductors (especially ZnO) tend to form poly- or nano-crystalline structures, which lead to the creation of grain boundary defects and therefore non-uniform TFT performance over larger areas.$^{88,115}$ Compared to binary compounds, multicomponent metal oxide semiconductors, in general, result in better TFT performance.$^{35,115}$ In multicomponents, a stable amorphous phase can be achieved by mixing two or more metal cations with different ionic charges and sizes, whereas the incorporation of a stabilizer metal cation can be used to better control the carrier concentration.$^{117}$ For example, IZO presents a stable amorphous phase, which leads to TFTs with good uniformity and $\mu$FE. Nevertheless, the high N > 10$^{17}$ cm$^{-3}$ leads to high $I_{OFF}$ and low $I_{ON}/I_{OFF}$. Given the stronger bonds of gallium (Ga) with O$_2$, indium gallium oxide (IGO) leads to a lower carrier density, but at the same time also smaller $\mu$FE.$^{35}$ To realize an amorphous oxide semiconductor with large $\mu$FE and $I_{ON}/I_{OFF}$, in 2004 Nomura et al. proposed the introduction of Ga into IZO, developing IGZO, the most widely used metal oxide semiconductor nowadays.$^{28}$ IGZO TFTs allow $\mu$FE > 10 cm$^2$ V$^{-1}$ s$^{-1}$ with N < 10$^{17}$ cm$^{-3}$.$^{28,115}$ Alternatives to Ga doping in IZO have also been developed, using tin (Sn), hafnium (Hf) and zirconium (Zr).$^{88,124-126}$ At the same time indium-free (and therefore cheaper) multicomponent metal oxide semiconductors (employing for example Sn, Al or Zr) have also been demonstrated.$^{54,88}$ Finally, also other multicomponent materials like ZnON have been reported.$^{127-130}$

Metal oxide semiconductors for flexible TFTs

Not all of the above mentioned metal oxide semiconducting materials have been employed as active layers in flexible TFTs.

Vacuum-processed metal oxide semiconductors

In the case of vacuum-processed flexible metal oxide semiconductor TFTs, amorphous IGZO is the most widely used material.$^{22,28,38,41,69,77,79-81,84,90,92,96,106,113,114,131-173}$ Flexible IGZO TFTs exhibit $\mu$FE up to 76 cm$^2$ V$^{-1}$ s$^{-1}$, depending on the stoichiometric composition employed. Also c-axis aligned crystalline (CAAC) IGZO TFTs on plastic foils have been demonstrated.$^{39,174,175}$ Crystalline ZnO, is the second most used metal oxide semiconductor in flexible TFTs, with $\mu$FE up to 50 cm$^2$ V$^{-1}$ s$^{-1}$.$^{59,78,176-182}$ Other metal oxide semiconducting materials used are: IZO with $\mu$FE up to
60 cm² V⁻¹ s⁻¹, 172,183–186 gallium zinc oxide (GZO) with μFE up to 20.7 cm² V⁻¹ s⁻¹, 187 and ZTO with μFE up to 14 cm² V⁻¹ s⁻¹. 64 Despite being considered a conductor in general, thin layers of indium tin oxide (ITO) can also be used, yielding μFE of 28.6 cm² V⁻¹ s⁻¹. 188

Solution-processed metal oxide semiconductors Most used solution-processed semiconductors are crystalline In2O3 and ZnO. For In2O3 TFTs, μFE up to 120 cm² V⁻¹ s⁻¹ have been reported, 76 including neat layers, nanoparticle (NP) or NW films, as well as blends of In2O3 and polyvinylpyrrolidone (PVP). 76,144,185–191 In the case of ZnO, the highest μFE values reached are of 7 cm² V⁻¹ s⁻¹. 192–194 Other solution-deposited metal oxide semiconductors include IZO with μFE around 4 cm² V⁻¹ s⁻¹, 195,196 ZTO with μFE of 0.04 cm² V⁻¹ s⁻¹ 197 and IGO with μFE of 0.4 cm² V⁻¹ s⁻¹. 198 Furthermore, solution-processed IGZO TFTs have shown excellent results with extremely high μFE values up to 84 cm² V⁻¹ s⁻¹, 83 either in the form of neat IGZO or in blends of IGZO and graphene nanosheets. 83,199,200

B. Flexible n-type vacuum-processed TFTs

In this subsection, the recent advances in the field of flexible n-type vacuum-processed metal oxide semiconductor TFTs are reviewed. In particular, the materials and the fabrication techniques employed will be first presented. Then, the electrical performance and the mechanical properties of the resulting devices will be discussed. Finally, additional features like dissolubility, mechanical activity, stretchability, and transparency will be tackled.

Materials: The materials needed for the fabrication of flexible n-type vacuum-processed TFTs include flexible substrates, conducting materials to realize the source/drain and gate electrodes, dielectric materials for buffer, passivation and/or insulating layers, and most importantly metal oxide semiconductor active layers.

Substrates: In contrast to standard Si MOSFET technology, the substrate used for the realization of TFTs is in general not a part of the active device itself, since it only provides a surface for the fabrication process. Nevertheless, the substrate, especially if flexible, has a significant influence on the final TFT properties, as well as on the manufacturing process. The key requirements concerning the substrate are:
(I) The surface has to be compatible with standard thin-film fabrication technology, which calls for roughness values in the nanometer regime.
(II) The melting or glass transition temperature (Tm or TG) of the substrate has to be high enough to be compatible with the chosen fabrication process.

(III) The substrate has to be bendable enough (in line with the mechanical requirements of the final devices), and at the same time has to provide sufficient stability for the manufacturing process.

(IV) The deformation of the substrate caused by temperature gradients, mechanical load, as well as absorption or desorption of gases or liquids during the fabrication has to be smaller than the minimum device feature size.

(V) Vacuum-processing techniques call for small outgassing rates, compatible with the available deposition tools.

(VI) Concerning a future mass production and commercialization, the substrates should be at least potentially available in large quantities and sizes, as well as cheap.

(VII) Furthermore, the substrate needs to be resistant to the chemicals used during the fabrication process, especially photoresists and developers.

(VIII) Finally, specific applications require substrates which are transparent, light-weight, conformable, stretchable, bio-compatible, and even biodegradable.

All these requirements have led to the evaluation of a large variety of different substrates. Due to their properties and their availability, polymers are the natural choice and the most commonly used substrate material. Among the different polymers, polyimide (PI) foils with thicknesses of t ≤ 5μm and 125μm are the most frequently utilized substrates, 134,144,151,156,157,159,164,171,176,179,183,187,188 together with PI and nano silica. 141,143 This is because of the numerous advantages of PI (commercially known as Kapton®), like a small coefficient of thermal expansion (CTE) of 12 × 10⁻⁶ K, a small humidity expansion coefficient (9 × 10⁻⁶ %RH), a high Tg of ≈360°C, and a surface roughness in the nanometer range. 114,154 Since standard PI exhibits a yellowish to brownish color, other polymeric substrates have been introduced to benefit from their transparency in the visible wavelength range. These materials, which are in general also cheaper and more easily available, include PET, 28,69,96,164,170,179,183,187 polyethylene naphthalate (PEN), 38,40,41,133,135,138,148,152,157,162,165–167,172,180,201 polyetheretherketone (PEEK), 202 polycarbonate (PC), 153,156 polypropylene (PP) based synthetic paper, 203 parylene, 80,140 polyethersulfone (PES), 177 water-soluble polyvinyl alcohol (PVA), 82 as well as polydimethylsiloxane (PDMS). 78,131,146,204–206 In particular, PDMS is also stretchable and biocompatible, but at the same time hard to process using standard fabrication techniques. 78,131,146,204 An alternative to polymers is constituted by metal foils, such as Al foils, 155 and stainless steel substrates. 147 The main benefit of metal foils is the high Tm (above 1000°C in the case of stainless steel). 154 Nevertheless, metallic substrates are conductive and thus require additional insulating buffer layers, which further increase weight and decrease flexibility. Other typologies of supports include flexible and transparent glass substrates compatible with high process temperatures. 159,173 glass-fabric reinforced
composites,\textsuperscript{93,168} cheap and biodegradable cellulose fiber-based paper,\textsuperscript{77,79,188,207} as well as nontoxic biological paper like beeswax.\textsuperscript{185} Additionally, also standard tracing paper (STP) and lab paper samples (LPS) with thickness between 51 µm and 75 µm have been employed. Finally, mechanically active multilayer substrates using a highly cross-linked hydrogel swelling layer and a stiff PI were also shown.\textsuperscript{22}

**Barrier layers:** Before starting the effective TFT fabrication, often buffer or encapsulation layers are deposited on top of the substrate itself. Although there are numerous examples of flexible n-type vacuum-processed metal oxide semiconductor TFTs manufactured without barrier layers, there are several reasons why an encapsulation of the substrate is beneficial, including:

(I) The need to electrically insulate a conductive substrate (e.g. Al or stainless steel).

(II) A reduction of the substrate surface roughness by the deposition of a smoothing layer.\textsuperscript{41}

(III) A reduction of the absorption and desorption of solvents during the fabrication process by decreasing the effective humidity expansion coefficient (HEC).

(IV) An improvement of the adhesion between the substrate and the device layers.

(V) A reduction of the substrate outgassing in low pressure environments to speed up the pumping steps during the deposition process.

(VI) A decrease of the substrate permeability by decreasing the effective water vapor transmission ratio (WVTR).

Typical adhesion or buffer layers are made of silicon nitride (\(\text{SiN}_x\)),\textsuperscript{92,106,113,114,139,142–145,149,150,172,181,182} silicon oxide (\(\text{SiO}_x\)),\textsuperscript{78,82,134,147,153,156,167,169,180,204} and photoresist sandwiched between \(\text{SiN}_x\) and \(\text{SiO}_x\).\textsuperscript{157} Organic materials,\textsuperscript{78,82,135,147,153,156,167,169,180,204} in particular SUS,\textsuperscript{152} or PVP are especially well-suited as smoothing layers.\textsuperscript{151,171} A direct comparison of the influence of different buffer layers (50 nm \(\text{SiO}_x\), 50 nm \(\text{SiN}_x\), or 50 nm \(\text{SiN}_x\) in combination with 10 nm or 100 nm \(\text{AlO}_x\)) on the performance of TG IGZO TFTs on PI substrate is given by Ok \textit{et al.}, as shown in Fig. 7.\textsuperscript{154} The buffer layer with the smallest WVTR (0.033 g/(cm²·day)) is given by 50 nm \(\text{SiN}_x\) + 100 nm \(\text{AlO}_x\). As shown by Ok \textit{et al.}, this buffer layer is able to reduce the carrier trapping at water related defects and results in the best device performance and stability (Fig. 7). Consequently several groups have published the use of multi-layers which can potentially combine the advantages of different materials. These layer stacks include organic TR-8857-SA7 with \(\text{Al}_2\text{O}_3\),\textsuperscript{138,201,203} undefined organic layers in combination with \(\text{Al}_2\text{O}_3\)\textsuperscript{93,166} as well as \(\text{SiO}_2\).\textsuperscript{40} The most complex published structure is a \(\text{SiO}_2/\text{SiN}_x/\text{SiO}_2/\text{SiN}_x/\text{SiO}_2\) sandwich layer,\textsuperscript{132,163} which could also be used to engineer the strain (\(\epsilon\)) in the stack, and other multi-stacked \(\text{SiO}_2/\text{SiN}_x\) barrier layers.\textsuperscript{136,176} Finally, 3 nm thick \(\text{SiO}_2\) were used as insulating encapsulation of conductive metal substrates.\textsuperscript{147}

**Gate dielectrics:** Together with the metal oxide semiconductor, also the gate dielectric plays a fundamental role. This is mainly due to the following reasons:

(I) As visible from equation I.1, the drain current \(I_D\) is directly proportional to \(C_{ox} = \frac{R_{ox}}{I_{ox}}\), where \(R_{ox}\) and \(t_{ox}\) are respectively the dielectric constant and the thickness of the gate dielectric. For low-voltage TFT operation, thin gate dielectric materials with high \(R_{ox}\) are desirable.

(II) The insulation properties, correlated with the specific resistance and the pinhole density (and therefore the layer deposition quality) of the dielectric material define the gate leakage of the device (the so called gate current \(I_G\)).

(III) The quality of the interface between the gate dielectric and the semiconductor can strongly influence the carrier mobility, as well as the stability of the TFT, by determining the interface trap density.

The most widely used gate dielectric is aluminum oxide in different forms, such as \(\text{Al}_2\text{O}_3\),\textsuperscript{22,41,59,80,81,93,96,144,146,161,168,177,178,182,201} \(\text{AlO}_x\),\textsuperscript{154} and also anodized \(\text{Al}_2\text{O}_3\) on Al gates.\textsuperscript{152,167} Additionally, anodic neodymium-doped \(\text{AlO}_x\) (\(\text{AlO}_x\):Nd)\textsuperscript{28,69} on aluminum neodymium (\(\text{AlNd}\)) gates has been used.\textsuperscript{157} The advantages of aluminum oxide are comparably high \(R_{ox}\) around 9.5, low pinhole density if deposited by atomic layer deposition (ALD), and, especially in combination with IGZO, a good interface quality. Employed materials with a higher \(R_{ox}\) include hafnium oxide (\(\text{HfO}_2\)),\textsuperscript{176,179,180} hafnium lanthanum oxide (\(\text{HfLaO}_3\)),\textsuperscript{169} titanium oxide (\(\text{TiO}_2\)),\textsuperscript{153} and yttrium oxide (\(\text{Y}_2\text{O}_3\)).\textsuperscript{28,69} The drawback of these dielectrics is a scarcer availability, a worst interface quality, as well as a worse compatibility with the TFT fabrication process. At the same time silicon oxide (either \(\text{SiO}_2\),\textsuperscript{40,78,132,136,137,147,162,163,165,172,173,187,204} or \(\text{SiO}_2\)) is a more established material, but results in a

![Figure 7. Transfer characteristics of flexible IGZO TFTs with 50 nm silicon nitride (\(\text{SiN}_x\))/10 nm aluminum oxide (\(\text{AlO}_x\)) (Device B), 50 nm \(\text{SiN}_x/100\) nm \(\text{AlO}_x\) (Device C), or 50 nm silicon oxide (\(\text{SiO}_x\)) (Device D) barrier layers on polyimide (PI) substrate. The inset shows a TDF (Device A) with a 50 nm \(\text{SiN}_x\) buffer layer. All measurements are done for pristine (dashed line) and 250 °C-annealed TFTs (solid line) (reproduced from Ok \textit{et al.} with permissions from AIP).\textsuperscript{154}](image-url)
Although the paper thickness is as high as 75 µm, even of a paper substrate as gate dielectric. Despite the use of TiO$_2$ and AlNd by Lim et al. showed that IGZO TFTs with SiO$_x$ dielectric exhibited slightly better performance than those with SiO$_2$. SiN$_x$ is only rarely used in the community. Besides metal oxide dielectrics, also organic materials have been used as gate dielectric, such as layers made from olefin polymers, or cross-linked PVP (c-PVP). To this regard, a direct comparison of c-PVP and SiO$_2$ showed that both materials have a comparable $\varepsilon_R$ and result in flexible IGZO TFTs with similar performance parameters, although the thick c-PVP layer ($t_{ox} = 280$ nm) reduces $C_{ox}$ if compared to the thinner SiO$_2$ ($t_{ox} = 170$ nm). A third class of gate dielectrics are ferroelectric materials, in particular poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)]. P(VDF-TrFE) can be reversibly polarized and hence used for the fabrication of non-volatile memory TFTs. Interestingly, recently also chicken albumen ferroelectric gate dielectrics have been demonstrated, as shown in Fig. 8. A fourth class of gate dielectric materials is constituted by solid electrolyte dielectric: (e.g. phosphorus (P)-doped SiO$_2$), which are characterized by high specific gate dielectric capacitance per unit area (C$_{ox}$) and therefore low-voltage device operation. This improvement is generally ascribed by a redistribution of mobile ions with the applied voltage. Fig. 9 illustrates how P-doped SiO$_2$ gate dielectrics allow achieving high C$_{ox}$ values of up to $13 \mu$F cm$^{-2}$. To combine the advantageous properties of different dielectric materials, a variety of hybrid and multi-layer materials have been utilized as gate dielectrics for flexible n-type vacuum-processed metal oxide semiconductor TFTs. These include: TiO$_2$ with HfO$_2$, PVP-Al$_2$O$_3$, or PVP with methylvyclohexane (pp-MCH) and Al$_2$O$_3$, SiN$_x$ with SiO$_2$, tri-layer stacks like TiO$_2$ sandwiched between SiO$_2$ or TiO$_2$ sandwiched between HfO$_2$, as well as P(VDF-TrFE) with Al$_2$O$_3$. Finally, an interesting approach is constituted by the use of a paper substrate as gate dielectric. Although the paper thickness is as high as 75µm, a $C_{ox}$ value of $4 \times 10^{-4}$ F m$^{-2}$ was achieved. This is because the dielectric properties are determined by an arbitrary serial and parallel combination of discrete fiber capacitors within the paper substrate. The large choice concerning possible dielectrics results in a big variety of published $C_{ox}$ values ranging from $1.2 \times 10^{-4}$ F m$^{-2}$ measured for an organic layer, up to $1.3 \times 10^{-1}$ F m$^{-2}$ for a solid electrolyte. Finally, ZnO was sandwiched between two layers of Al$_2$O$_3$ to create a charge trapping layer in the gate oxide, leading to non volatile memory TFTs.

**Contacts:** This class of materials includes metals and other conductors employed to fabricate gate and source/drain electrodes. Since the gate contact of a TFT (and in general of a FET) does not need to conduct a significant amount of current, the material is in general selected to achieve a high compatibility with the TFT fabrication process. This issue was also addressed by a direct comparison between different gate metals like chromium (Cr), titanium (Ti), copper (Cu), and platinum (Pt). Fig. 10 displays the corresponding transfer characteristics showing that although the work function of the various gate metals is different, their influence on the electrical performance of IGZO TFTs is minor. Consequently a variety of different metals: silver (Ag), Al, Au, Cr, Cu, Ni, Pt, Ti, molybdenum (Mo), molybdenum titanium (MoTi), and nickel (Ni), as well as AlNd, molybdenum titanium (MoTi), molybdenum.
and tantalum nitride (TaN) metal alloys have been used as gate contacts.\textsuperscript{153,156,169} Especially for BG TFTs, the adhesion of the gate contact to the flexible substrate appears to be the main concern. To this aim, Cr and Ti show good results, whereas Cr often suffers from a high built-in strain.\textsuperscript{90} Multi-layer metal contacts are used in general a compromise between good adhesion and high conductivity, especially in the case of Ti/Au,\textsuperscript{22,96,180} Ti/Cu,\textsuperscript{134} Cr/Au,\textsuperscript{173} or Ti/Au/Ti gate stacks.\textsuperscript{161} Besides metals and metal alloys, ITO,\textsuperscript{28,69,78,80,138,164,176,179,183,187,204} IZO,\textsuperscript{77,79,132,134,139,167,179,183,187,204} In\textsubscript{2}O\textsubscript{3},\textsuperscript{170} and aluminum zinc oxide (AZO) were used to fabricate transparent gate contacts.\textsuperscript{93,133} Furthermore, dual-layers of metal and ITO,\textsuperscript{40} or IZO have also been employed.\textsuperscript{141} As regards source/drain electrodes, the material has to provide a high conductivity and at the same time a small contact resistance with the active layer. Moreover, also other properties like adhesion or transparency need to be considered. These requirements resulted in the use of different metals: Al,\textsuperscript{77,148,151,153,156,164,169,171,178,207} Au,\textsuperscript{38,166} Cu,\textsuperscript{146} Mo,\textsuperscript{41,82,136,137,147,163,167} palladium (Pd),\textsuperscript{144} and Ti,\textsuperscript{90,93,143,168} whereas Mo and Ti seem to exhibit the lowest specific contact resistance R\textsubscript{C}. At the same time, a big variety of multi-layer contacts were developed to combine the advantageous properties of different materials: recent examples are: Ti/Au,\textsuperscript{59,69,81,84,113,139,140,142,145,149,150,180–182} Ni/Au,\textsuperscript{79} Mo/Al,\textsuperscript{165,172} Cr/Au,\textsuperscript{114} Mo/AlN,\textsuperscript{155} Cr/Au/Cr,\textsuperscript{92} Mo/Al/Mo,\textsuperscript{152} Ti/Au/Ti,\textsuperscript{161} or Ti/IZO.\textsuperscript{141} Regarding transparent source/drain contacts, only ITO,\textsuperscript{28,78,80,106,138,154,157,176,179,187,188,201,203,204} and IZO have been used.\textsuperscript{159,170,183} Finally, contacts based on Ti (drain) and graphene (source) in combination with a VTFT structure have been published.\textsuperscript{96}

**Passivation layers:** The performance of BG TFTs can be improved by depositing a final back channel passivation layer. This can lead to the following advantages: (I) An increase of the environmental and electrical stability of the TFTs by a reduced interaction between semiconductor and atmosphere (in particular less interaction of the active layer with oxygen and water). (II) An encapsulation of the TFTs from a mechanical point of view. (III) A protection of the devices during post-processing steps like the fabrication of additional devices, such as organic light emitting diodes (OLEDs) or touch screens. To simplify the fabrication process, it is quite common to passivate the device using the same material already used for the gate dielectric. Furthermore, Al\textsubscript{2}O\textsubscript{3} passivation layers are widely used because of the low oxygen transmission rate (OTR) of \(\approx 1.26 \times 10^{-4} \text{mol/(m}^2\text{day)}\) and WVTR rate of \(\approx 6.61 \times 10^{-2} \text{mol/(m}^2\text{day)}\) (both measured for a 8 nm thick Al\textsubscript{2}O\textsubscript{3} layer on PET).\textsuperscript{90} Al\textsubscript{2}O\textsubscript{3} passivation layers result in BG metal oxide semiconductor TFTs with significantly improved stability, compared to unpassivated devices.\textsuperscript{80,81,113,114,139,142,149,150,178} For similar reasons, also SiO\textsubscript{2},\textsuperscript{163,165,167,172} SiO\textsubscript{x},\textsuperscript{132,155} and TiO\textsubscript{2} have been used.\textsuperscript{156} Additionally, organic layers such as photoresist,\textsuperscript{103,152} SUS,\textsuperscript{78,157,204} tetratetracontane,\textsuperscript{151} and polychloroprene in combination with Al\textsubscript{2}O\textsubscript{3} have been utilized to passivate flexible n-type vacuum-processed metal oxide semiconductor TFTs.\textsuperscript{22}

**Fabrication techniques:** The fabrication of flexible n-type vacuum-processed metal oxide semiconductor TFTs employs standard semiconductor fabrication tools. Nevertheless, the large variety of available substrates with different physical and chemical properties has led to the use of a wide range of different techniques. These include several approaches to handle the flexible substrates, as well as to deposit and structure the various device layers.

**Substrate preparation:** The substrate choice for example limits the maximum allowed temperature, as well as the list of chemicals that can be used during the fabrication process. At the same time, the mechanical properties of the flexible support also determine the way how the substrate can be handled. Up to now, free-standing flexible substrates are widely employed.\textsuperscript{93,96,133,144,153,155,156,164,171,177,179,183,187,188,208} Free-standing foils are a natural choice for the fabrication of flexible devices because they are compatible with large scale substrates and they also represent a step towards future roll-to-roll processes. Furthermore, the mechanical robustness of free-standing foils results in an insensitivity against mechanical shocks. At the same time free-standing substrate also present drawbacks: (I) They have to be sufficiently thick and stable to be mechanically handled with tweezers. (II) They can suffer from expansion caused by temperature gradients or by the absorption of solvents. (III) They have to be temporarily attached to a rigid carrier at least during the use of standard photolithographic tools.
One way to simplify the use of photolithographic tools like mask aligners or spinners is to bond the flexible foil to a glass or silicon wafer for the complete fabrication process. An alternative, a flexible foil can also be mechanically fixed on particularly designed holders using metallic clamps. An alternative to flexible substrates manufactured independently from the TFTs, it is also possible to create the flexible substrate by covering a host substrate with a polymer using either evaporation, spin, slot or blade coating techniques. The advantages of these fabrication techniques based on a rigid support are a high compatibility with the standard fabrication processes on Si or glass wafers, a reduction of the expansion of the substrate during the manufacturing process, as well as the possibility to realize devices on very thin (≈1 μm) substrates. After the TFT fabrication is completed, the flexible foils or thin deposited polymer layers carrying the devices are either removed mechanically, by the use of a low adhesion releasing layer, or by employing a sacrificial layer between the host carrier and the polymer. 

To this regard a direct comparison of different releasing methods by Lin et al. showed that mechanical peeling of the flexible substrate from the hosting carrier wafer can lead to deformation and cracking of the TFTs in case of high adhesion forces between the polymer and the carrier. To increase the mechanical stability, or to realize electronic devices on alternative surfaces, thin flexible substrates are also transferred and attached to a new carrier like PI or organic tissues. Finally, it is also possible to fabricated TFTs directly on a rigid carrier coated with a sacrificial layer and subsequently transfer only the devices onto a flexible substrate. In addition to the different handling possibilities, the substrate preparation also includes a heat treatment step prior to the device fabrication itself. In the case of fabrication on free-standing plastic foil or foil bonded to a host substrate, the substrate is backed at high temperatures (around 200 °C) for several hours, to remove trapped residual liquids. This step allows also pre-shrinking flexible substrates which are not permanently attached to a rigid support.

Deposition methods: Besides the standard criteria used for thin-film deposition techniques on Si or glass wafer (e.g. homogenous and dense layers), there are extra requirements which are especially important for the realization of flexible devices. These include:

(I) Low temperatures, compatible with the thermal resistance of the employed flexible substrates.

(II) A sufficient adhesion of the deposited materials to the substrate, in order to prevent a possible delimitation of the layers, especially when the substrate is bent. (III) Finally, the strain built in the deposited materials has to be small enough to allow good mechanical properties (e.g. bendability) of the final devices.

The predominant technique to deposit n-type vacuum-processed metal oxide semiconductors is sputtering. The advantages of sputtering are the low temperature (typically room-temperature) deposition, as well as the good adhesion and dense structure of the final layers. Additionally, sputter tools offer several opportunities to optimize the layer properties, by adjusting the power and/or the sputtering pressure. Also reactive sputtering using different concentrations of Argon (Ar) and O2 has been used to adjust the oxygen content in the metal oxide semiconducting active layer. An even better control of the stoichiometric composition of IGZO is possible by using co-sputtering techniques based on an IZO and a Ga2O3 target. Among all the n-type metal oxide semiconductors, ZnO is the only one that can be deposited by ALD, plasma enhanced atomic layer deposition (PEALD), and PLD. Even if ALD has the advantage that the layers are conformal, the process is slow and any variation of the chemical composition can be hardly achieved.

The deposition of insulating layers to realize gate dielectrics, passivation, or barrier layers aims at a high $\varepsilon_R$, a low pinhole density and a good sidewall coverage. This is why, conformal deposition techniques are particularly well-suited: ALD, PEALD of Al2O3, ALD of HfO2 as well as plasma-enhanced chemical vapor deposition (PECVD) of SiO2, SiN, SiO2:P, and PLD. These depositions are in general done at temperatures between 150 °C and 200 °C. Sputtering also results in comparably conformal layers, and has therefore been used to deposit Y2O3, SiO2, HfO2, and HfO2 whereas PLD has only been employed to grow Y2O3. Although evaporation of metal oxides requires high temperatures, different dielectrics (Al2O3, HfLaO, SiO2, TiO2, and HfO2) have been deposited by electron-beam evaporation. Besides the mentioned vacuum-deposition techniques, high-quality Al2O3 and Al2O3:Nd gate dielectrics have also been grown anodizing a metallic gate. Finally, organic layers, in particularly PVP, chicken albumen, or P(VDF-TrFE) have been spin coated.
Metals are typically deposited using e-beam evaporation, thermal evaporation, or sputtering. Non metallic but transparent metal oxides have been fabricated by sputtering (ITO), by e-beam evaporation of AZO and IZO, or by PLD (ITO). It is worth mentioning that also graphene monolayers grown by chemical vapor deposition (CVD) and transferred to a flexible PET substrate can be employed, as reported by Liu et al. Some of the presented deposition procedures (e.g. from Li and Jackson, or Cherenack and Tröster) are designed in a way that the semiconductor and the gate dielectric can be deposited with the same tool. In this way, it is possible to avoid the surface contamination caused by breaking the vacuum and transferring the sample to another tool. However, there is no clear evidence in literature that breaking the vacuum necessarily leads to a degenerated device performance.

Layer structuring: As for the structuring of layers on rigid wafers, patterning of thin-films on flexible substrates is mainly done by etching and lift-off processes. However, the definition of flexible structures needs to be adapted to the mechanical and chemical properties of the substrates. Since the most common substrates, in particular PI foils, are resistant to standard photolithographic chemicals, UV lithography is widely used. Employing etching and lift-off processes allows realizing flexible structures with lateral feature size down to 1 µm. If the chosen substrate is not resistant to chemicals (e.g. photoresists, developers and/or strippers) and if feature sizes ≫ 1µm are sufficient, shadow masking can be used. Shadow mask structuring does not require any photoresist baking step and allows therefore preventing unintended annealing of the devices, as well as undesired thermal load of the substrate leading to subsequent expansion. The problem of substrate expansion is illustrated by the fact that a 7.6 cm × 7.6 cm large PI substrate undergoes an expansion of ≈25 µm (in each direction) during a 150°C TFT fabrication process. Due to this expansion, tolerances of ≈10µm on the photolithographic masks are necessary, limiting thus the minimum feature sizes that can be achieved. In particular, special care needs to be taken during the alignment of the source/drain contacts to the gate electrode, which can result in large total overlap lengths L_{OV,TOT} and therefore low transit frequency f_T (see Equation I.8). The problem of source/drain contacts misaligned with respect to the gate electrode is practically shown in Fig. 11 for a flexible IGZO TFT. A solution to misalignment caused by thermally-induced substrate expansion is constituted by self-aligned lithography. Due to the transparency of the majority of flexible substrates, the photoresist can be structured using back-side exposure and predefined opaque patterns (e.g. metallic BG contacts). In this way, there is no need for tolerances on the photolithographic masks and feature sizes down to 0.5µm are possible. Fig. 11 displays a direct comparison of TFTs fabricated using standard and self-aligned lithography. Furthermore, self-alignment is also possible by using a metallic top gate contact as mask to structure the gate insulator in a RIE process. This approach has the additional advantage that the RIE plasma increase the conductivity of the used IGZO semiconductor in the contact areas. A similar effect can be achieved by depositing SiNx using PECVD. Here, a top gate protects the channel while the SiNx deposition increase the conductivity of IGZO and thereby forms self-aligned source and drain contacts close by.

Device configuration: For flexible n-type vacuum-processed metal oxide semiconductor devices, the four main TFT configurations (see I B) have been employed:

(I) The most common TFT geometry is the BG, (II) TG structures are utilized especially if fragile gate dielectrics that do not survive extensive processing and/or chemicals (e.g. P(VDF-TrFE)) are employed, (III) DG TFTs are used to improve the TFT DC performance, as well as the device environmental stability.
Electrical properties: One of the main reasons why flexible n-type vacuum-processed metal oxide semiconductor TFTs have received an increasingly amount of attention in the last years is their electrical performance, which is superior to other flexible TFT platforms, especially organic and a-Si technologies (see Table I). A typical transfer and output characteristic of a flexible n-type vacuum-processed metal oxide semiconductor TFT (in this case based on IGZO) is plotted in Fig. 12. The DC performance parameters of the shown device are given in the figure caption. The best DC performance parameters ever reported for flexible n-type vacuum-processed metal oxide semiconductor devices include: a $\mu FE$ of 76 cm$^2$/V·s, a threshold voltage $V_{TH} = 1.0$ V, a sub-threshold swing $SS = 102$ mV/dec, and current on/off ratio $I_{ON}/I_{OFF} = 9.5 \times 10^5$, resulting in a specific transconductance $g_{m}/W$ (at $V_{GS} = 5$ V) of $2.02$ S·m$^{-1}$. (IV) Finally, also flexible VTFTs (Fig. 4e) and QVTFTs with short channel lengths (down to 300 nm) and reduced device footprint have been presented.

Device optimization: Numerous techniques have been proposed to improve the electrical performance of flexible n-type vacuum-processed metal oxide semiconductor TFTs, ranging from material and process engineering to device structure modifications. Table II presents an overview of the performance of recently published flexible n-type vacuum-processed metal oxide semiconductor TFTs. Each of the devices shown in Table II yields at least one of the best performance parameters ever reported for flexible n-type vacuum-processed metal oxide semiconductor TFTs. These results have been possible thanks to several optimization approaches:

(I) The probably simplest way to influence the de-
vice performance is to expose the TFTs to elevated temperatures either during or after the fabrication process. Annealing at or around 200 °C is a common way,40,82,131,133–136,151,152,154,155,157,159,164,167,207 whereas temperatures above 260 °C,158 are not possible due to the thermal properties of the majority of the (polymeric) substrates. Nevertheless, flexible glass and metal substrates allow higher annealing temperatures of 300 °C,155,159 330 °C,204 and even 400 °C.173 An investigation of the influence of annealing on e-beam evaporated TiO2 gate dielectrics showed that, for annealing temperatures below 200 °C, the I off on only weakly depends on the temperature, but decreases by approximately one order of magnitude if the annealing temperature is increased to 300 °C.153 Besides traditional post-deposition annealing of thin-films, also the deposition of metal oxide semiconductors at high temperatures influences the performance. Fig. 14 shows TFTs based on IGZO deposited at elevated temperatures.167 In this case, sputtering of IGZO at 150 °C results in slightly higher μFE compared to untreated or post-annealed (at 150 °C) TFTs. Nevertheless, while increased temperatures definitely improve the performance167 and the stability of single TFTs,152,159 there is no clear trend showing that annealed TFTs always exhibit better performance (e.g. higher μFE) than non-annealed one. One explanation could be the fact that TFTs are often exposed to an indirect annealing at elevated temperatures during the fabrication process (e.g. during the deposition of passivation layers at high temperatures around 150 °C).113,178 The same trend also applies for room-temperature fabricated devices with unspecified temperatures employed during the photolithographic steps.28,77,153,180,187 Even TFTs fabricated by shadow masking by Erb et al. with at least two elevated temperature steps during and after the IGZO deposition resulted in reasonable μSAT and Ion/Ioff of 4.6 cm2 V−1 s−1 and 1 × 108, respectively.161 A more uncommon approach was used by Park et al., who significantly increased the μFE of ZnO TFTs (from 0.2 cm2 V−1 s−1 to 1.5 cm2 V−1 s−1) by using microwave annealing at a frequency of 2.45 GHz, and a power of 700 W for 15 min.177 (II) Another effective way to improve the TFT performance and stability is the optimization of the semiconductor that can be realized adjusting the oxygen content in the sputter atmosphere and/or employing dual-layer semiconductors. Flexible GZO TFTs for example exhibit an optimized current on/off ratio if an oxide content of 25% is used during the semiconductor deposition.187 A study by Nag et al. showed how TFTs with dual-layers of IGZO with different thicknesses and different amounts of O2 allow precisely controlling the charge carrier density.41 In this case, TFTs with dual-layers (7 nm IGZO with 0% O2/15 nm IGZO with 5% O2) resulted in enhanced performance, if compared to devices with 20 nm single-layer of IGZO.41 At the same time, an increased temperature on the fabrication process (e.g. during the deposition of passivation layers) could be the fact that TFTs are often exposed to an indirect annealing at elevated temperatures during the fabrication process. Annealing at or around 200 °C is a common way,40,82,131,133–136,151,152,154,155,157,159,164,167,207 whereas temperatures above 260 °C,158 are not possible due to the thermal properties of the majority of the (polymeric) substrates. Nevertheless, flexible glass and metal substrates allow higher annealing temperatures of 300 °C,155,159 330 °C,204 and even 400 °C.173 An investigation of the influence of annealing on e-beam evaporated TiO2 gate dielectrics showed that, for annealing temperatures below 200 °C, the I off on only weakly depends on the temperature, but decreases by approximately one order of magnitude if the annealing temperature is increased to 300 °C.153 Besides traditional post-deposition annealing of thin-films, also the deposition of metal oxide semiconductors at high temperatures influences the performance. Fig. 14 shows TFTs based on IGZO deposited at elevated temperatures.167 In this case, sputtering of IGZO at 150 °C results in slightly higher μFE compared to untreated or post-annealed (at 150 °C) TFTs. Nevertheless, while increased temperatures definitely improve the performance167 and the stability of single TFTs,152,159 there is no clear trend showing that annealed TFTs always exhibit better performance (e.g. higher μFE) than non-annealed one. One explanation could be the fact that TFTs are often exposed to an indirect annealing at elevated temperatures during the fabrication process (e.g. during the deposition of passivation layers at high temperatures around 150 °C).113,178 The same trend also applies for room-temperature fabricated devices with unspecified temperatures employed during the photolithographic steps.28,77,153,180,187 Even TFTs fabricated by shadow masking by Erb et al. with at least two elevated temperature steps during and after the IGZO deposition resulted in reasonable μSAT and Ion/Ioff of 4.6 cm2 V−1 s−1 and 1 × 108, respectively.161 A more uncommon approach was used by Park et al., who significantly increased the μFE of ZnO TFTs (from 0.2 cm2 V−1 s−1 to 1.5 cm2 V−1 s−1) by using microwave annealing at a frequency of 2.45 GHz, and a power of 700 W for 15 min.177 (II) Another effective way to improve the TFT performance and stability is the optimization of the semiconductor that can be realized adjusting the oxygen content in the sputter atmosphere and/or employing dual-layer semiconductors. Flexible GZO TFTs for example exhibit an optimized current on/off ratio if an O2 content of 25% is used during the semiconductor deposition.187 A study by Nag et al. showed how TFTs with dual-layers of IGZO with different thicknesses and different amounts of O2 allow precisely controlling the charge carrier density.41 In this case, TFTs with dual-layers (7 nm IGZO with 0% O2/15 nm IGZO with 5% O2) resulted in enhanced performance, if compared to devices with 20 nm single-layer of IGZO.41 At the same
time, if compared to single-layer TFTs, dual-layer IGZO devices exhibit also improved stability, as displayed in Fig. 15. Dual-layers of IZO deposited in gradient O₂ ambient have been used to fabricate semiconducting (4% or 7% O₂) and low resistance IZO layers (0% O₂). The resulting flexible TFTs (Fig. 16) show a strong dependency of the μFE and VTH on the sputtering conditions. Finally, Marrs et al. demonstrated flexible dual-layer TFTs (with IGZO at the interface with the dielectric and with highly doped IZO close to the source/drain contacts) yielding improved stability and mobility.

(III) Also the choice of the gate dielectric plays a key role in the TFT optimization, by directly influencing the specific gate dielectric capacitance (and therefore also the drain current and the sub-threshold swing) of the device. One possibility to improve Cox is the use of multi-layer gate dielectrics with good interface quality, such as HfO₂/TiO₂, PVP/TiO₂, SiO₂/SiNx and HfO₂/TiO₂/HfO₂. Another approach to increase the Cox while keeping the advantageous interface properties of Al₂O₃ is the use of thin (10 nm) Al₂O₃ grown by ALD. Additionally, ferroelectric gate dielectrics, either P(VDF-TrFE) or Al₂O₃ in combination with chicken albumen, can be used to generate a gate hysteresis of up to several volts in the TFT transfer characteristics. Fig. 17 displays the transfer curve of a flexible IGZO TFT with Al₂O₃/P(VDF-TrFE) gate dielectric, showing how the gate hysteresis allows realizing a non-volatile 1-bit memory element. (IV) The use of a suitable passivation layer can lead to TFTs with enhanced stability, as well as performance. A direct comparison of TFTs with and without a TiO₂ passivation layer was published by Hsu et al. Hsu et al. showed that a TiO₂ capping layer on BG IGZO TFTs increases the μFE from 10 cm²V⁻¹s⁻¹ to 61 cm²V⁻¹s⁻¹. Such improvement was attributed to a larger electron accumulation caused by a higher electric field under the high-ε TiO₂ capping layer. (V) Even if the barrier layer has no direct impact on the TFT performance, its barrier and surface properties can influence the final device. TFTs with SiO₂, SiNx, or SiNx in combination with AlOₓ (10 nm or 100 nm) buffer layer have been compared by Ok et al. In their work, Ok et al. show that SiNx/AlOₓ dual-layer barriers yield better water and hydrogen diffusion barriers and therefore improved device performance, if compared to TFT with single buffer layers (SiNx or SiO₂). Similarly, flexible IGZO TFTs fabricated on PEN using 3µm organic TR-8857-SA7 + 50 nm Al₂O₃ dual-layer resulted in superior performance compared to those manufactured on PET with a single 3µm thick TR-8857-SA7 layer or without buffer layer.

(VI) Finally, the device geometry can be adjusted...
Figure 18. Flexible DG IGZO TFTs: a) Total gate capacitance ($C_G$), and ratio between the $C_G$ of a DG TFT and the corresponding BG reference TFT and b) transconductance ($g_m$) of DG and BG TFTs for different values of the over-bias voltage ($V_{GS}-V_{TH}$). The insets in a) and b) show the measurement setup and the DG device cross-section, respectively (adapted from Münzenrieder et al. with the permissions from Elsevier). \cite{90}

to achieve significant improvements in the electrical performance. First, it is worth mentioning that BG TFTs (Fig. 4a-b) provide a generally better performance if compared to TG devices (Fig. 4c-d). Indeed, the average $\mu_{FE}$ of all the flexible n-type vacuum metal oxide semiconductor BG TFTs cited in this subsection is 16.6 cm$^2$V$^{-1}$s$^{-1}$, while the corresponding value for TG devices is only 12.7 cm$^2$V$^{-1}$s$^{-1}$. Although this comparison is not entirely valid since the values are not normalized for the different channel materials etc., these two average numbers highlight the better interface quality of BG TFTs, compared to TG ones. On the other side, DG architectures (Fig. 4e) exhibit a by a factor of $\approx 2$ larger effective gate area,\cite{90,106} which results in a total gate capacitance increased by the same factor, as shown in Fig. 18. The increased gate capacitance $C_G$ leads to a larger transconductance $g_m$, as demonstrated in Fig. 18b, where flexible DG and BG IGZO TFTs are compared. Since $g_m$ and $C_G$ increase simultaneously, there is no significant effect on the TFT AC performance (see equation I.8).\cite{106}

Nevertheless, DG structures also influence the threshold voltage, and the increased $C_G$ enabled the smallest published SS of 69 mV/dec.\cite{90} DG architectures present also an increased effective gate to source/drain overlap and hence reduced $R_C$ from 205 kΩμm to 165 kΩμm (if compared to the corresponding BG TFT reference structures).\cite{106} Furthermore, the $\mu_{FE}$ of DG TFTs can be either reduced (because of more interface scattering caused by additional process steps, and therefore less clean interfaces) or increased (because of less interface scattering caused by the reduced lateral electric field) if compared to the corresponding BG TFTs.\cite{106} Which of these effects is dominant varies across literature. To realize fast and flexible TFTs, devices with small feature sizes (especially short channel lengths), need to be fabricated. Since the realization of short channels on flexible substrates can be challenging, two alternative concepts based on vertical device geometries have been developed: flexible metal oxide semiconductor VTFTs (Fig. 4f),\cite{92,93,96} and QVTFTs.\cite{144} Both device structures are characterized by the fact that the channel is oriented out of the plane with respect to the substrate.\cite{144} This is realized by depositing an insulating layer between the source and the drain contacts (the so called spacer), whose thickness defines the channel length. Thereby channels as short as 300 nm are possible.\cite{144} Unfortunately, VTFTs and QVTFTs suffer from a bad interface quality, high contact resistance and large overlap capacitance.\cite{92,144} Therefore, only transit frequencies below 1.5 MHz have been possible with such vertical structures.\cite{92,144} Nevertheless, VTFTs have great potential for applications where a small footprint is required. Flexible n-type vacuum-processed metal oxide semiconductor TFTs with both short channels and small overlap capacitance have been manufactured using self-alignment techniques. In particular, flexible self-aligned IGZO TFTs ($L = 500$ nm and $L_{OV,S} = L_{OV,D} = L_{OV} = 1.55$ μm) enabled the realization of the highest $f_T$ of 135 MHz (see Fig. 13) ever reported for flexible metal oxide semiconductor devices.\cite{144,208} The same self-alignment approach was also used to fabricate flexible DG IGZO TFTs with two self-aligned gates ($L = 7.5$ μm and $L_{OV} = 1$ μm), yielding an $f_T$ of 5.6 MHz.\cite{106} The influence of the channel scaling, together with the use of different source/drain to gate overlaps is shown in Fig. 19. The graph displays the transit frequency (extracted from S-parameter measurements) of flexible IGZO TFTs fabricated with conventional lithography ($L_{OV}$ of 15 μm and 5 μm) and self-alignment ($L_{OV} = 1.5$ μm). The positive effect of the reduced device dimensions is evident. At the same time, Fig. 20 shows how the overlap length-dependent contact resistance of TFTs limits the impact of further channel scaling on the device $f_T$. Therefore significantly higher frequency values call for a reduction of the specific contact resistance.\cite{208}

**Modeling:** Besides the optimization of the electrical properties itself, it is also important to model the TFT behavior prior to the fabrication. Device modeling is not only essential for the design and simulation of com-
the model presented by Zysset et al. is that is that no testing on the channel scaling has been provided. A more complete model was presented by Perumal et al., who reported the simulation of flexible IGZO TFTs based on a level 3 HS pice level 3 model (reproduced from Perumal et al. with permissions from IEEE). The drawback of the model is that the electrical characteristics, but needs to deal also with the mechanical properties. To fully describe the mechanical properties of flexible n-type vacuum-processed metal oxide semiconductor TFTs, issues like induced strain, maximum strain resistance, influence of strain on the electrical properties, as well as role of mechanical fatigue need to be thoroughly addressed.

**Bendability:** Bending is the most common technique employed to induce strain in flexible TFTs. This is mainly because bent thin-film devices enable many applications like rollable displays, smart labels, seamless and embedded patch-like systems, electronic textiles, and implantable electronic devices for medical equipment. While rollable displays, smart labels, as well as embedded patch-like systems can be realized using flexible TFTs with minimum bending radii in the model presented by Zysset et al., who proposed a level 61 HS pice level 3 model (reproduced from Perumal et al. with permissions from IEEE).

**Mechanical properties:** A complete set of performance parameters of flexible TFTs cannot be limited to the electrical characteristics, but needs to deal also with the mechanical properties. To fully describe the mechanical properties of flexible n-type vacuum-processed metal oxide semiconductor TFTs, issues like induced strain, maximum strain resistance, influence of strain on the electrical properties, as well as role of mechanical fatigue need to be thoroughly addressed.

**Bendability:** Bending is the most common technique employed to induce strain in flexible TFTs. This is mainly because bent thin-film devices enable many applications like rollable displays, smart labels, seamless and embedded patch-like systems, electronic textiles, and implantable electronic devices for medical equipment. While rollable displays, smart labels, as well as embedded patch-like systems can be realized using flexible TFTs with minimum bending radii in

Figure 19. Transit frequency $f_T$ of flexible IGZO TFTs with different values of channel length ($L$) and total overlap length between gate and source/drain ($L_{OV}$) fabricated by conventional ($L_{OV}$ of 15µm and 5µm) and self-aligned ($L_{OV}$ of 1.5µm) lithography. The inset displays the geometrical parameters (adapted from Münzenrieder et al. with permissions from AIP and IEEE).  

Figure 20. Channel and overlap length-dependent calculation of the transit frequency of flexible IGZO TFTs (verified by S-parameter measurements): the calculation for a real TFT includes the influence of the parasitic overlap capacitance ($C_{OV}$) and the contact resistance ($R_C$), as compared to the ideal case (no $C_{OV}$ and $R_C$ considered). The extrapolation to short channel lengths shows the dominant influence of contact resistance on the TFT transit frequency (adapted from Münzenrieder et al. with permissions from AIP).

Figure 21. Flexible IGZO TFTs: measured output characteristic (average of four TFTs with W/L = 50µm/50µm) and corresponding curve simulated with a HS pice level 3 model (reproduced from Perumal et al. with permissions from IEEE).
the centimeter range, smart electronic textiles call for much smaller radii in the sub-millimeter regime.\cite{213} On the other side, medical applications need thin-film devices that can adapt to the human body, e.g. to a human hair which exhibits a radius of $\approx 50\mu m$. Flexible n-type vacuum-processed metal oxide semiconductor TFTs, especially based on IGZO active layers, bent to different radii have been characterized by many research groups.\cite{39,80,96,106,131–134,138,143,144,151–160,178–180,183,203,207,214}

As illustrated in Fig. 22a, mechanical bending tests are in general performed by winding the flexible TFT substrate around cylindrical rods. At the same time, some research groups have also developed automated bending testers like the one shown in Fig. 22b, which can be used to perform multiple bending and re-flattening cycles,\cite{132,136,138,151,152,160,178,214} as well as to characterize the TFTs at arbitrary bending radii while the devices are connected to a parameter analyzer.\cite{149} The approach based on the bending tester allows carefully controlling the applied strain during the entire measurement, and in some cases also ensures a permanent and reliable contact between the TFT and the characterization equipment. Independently of the measurement setup, flexible n-type vacuum-processed metal oxide semiconductor TFTs can be bent down to $50\mu m$ in the case of tensile (outward) bending,\cite{80} and down to $25\mu m$ for compressive (inward) bending.\cite{22} Nevertheless, it has to be mentioned that, because of difficulties in contacting the devices while being inward bent, bending in compressive direction is not very common. As visible from Table II, the maximum strain values do not only depend on the minimum bending radii, but also on the device layers and thicknesses. Since the calculation of the mechanical strain in a multi-layer system can be complex, different equations have been used to estimate numerical values of the strain induced by bending. One of the most common approximations is the following:\cite{215}

$$
\epsilon = \left(1 - \frac{1}{R} \right) \left(1 - \frac{1}{R_0} \right) \times \frac{t_S + t_D}{2} \times \frac{Y_S}{Y_D} \left(\frac{t_D}{t_S}\right)^2 + 2 \frac{Y_S}{Y_D} \frac{t_D}{t_S} + 1
$$

(II.1)

where $R$ is the bending radius, $R_0$ is the initial bending radius caused by the built-in strain (has to be added if the built-in strain is in the opposite direction as the induced strain, elsewhere subtracted), $t_D$ is the thicknesses of the device, and $Y_S$ and $Y_D$ are the Young’s moduli of the substrate and the device, respectively. The highest strain values at which flexible n-type vacuum-processed metal oxide semiconductor TFTs have been able to operate include $1.89\%$,\cite{138,201} (tensile direction) and $-0.6\%$ (compressive direction).\cite{145} In addition to one-time bending tests, also the TFT resistance to mechanical fatigue caused by repeated bending and re-flattening cycles was investigated. In particular, tensile bending cycles up to $100,000$ have been reported,\cite{136,151} while repeated compressive bending tests have been limited to $24$ cycles.\cite{150} While the majority of the published bending measurements only confirmed the functionality of the devices at a given bending radius or after repeated bending cycles, other more sophisticated experiments focused on the influence of strain on the electrical TFT performance. In the majority of the cases (for IGZO TFTs), bending resulted in an increase of the drain current under tensile bending, and in a decrease of the drain current under compressive strain. At typical tensile strain ($\epsilon \approx 0.5\%$), the $I_D$ changes are caused by an increase of the $\mu_{FE}$ by $\approx 2.5\%$ and by a decrease of the $V_{TH}$ by $\approx 20mV$ to $200mV$. At the same time, compressive strain ($\epsilon \approx 0.5\%$) causes $\mu_{FE}$ and $V_{TH}$ changes around $\approx -2\%$ and $\approx 10mV$ to $150mV$, respectively.\cite{84,90,143,147,149,150,155,171} The opposing effect of tensile and compressive bending on the DC performance of flexible IGZO TFTs is visualized in Fig. 23. Furthermore, also the influence of repeated cycles of bending and re-flattening on the characteristics of flexible IGZO TFTs (measured while flat) has been analyzed.\cite{150} The effect of long-term bending depends on the repetition duration.\cite{150} Nevertheless, bending cycles nearly always lead to a decreased $I_D$, probably due to the formation of micro-cracks on a short time scale (already after $24$ bending cycles).\cite{150} However, also cyclic tensile/compressive bending results in parameter shifts similar to those observed for tensile/compressive one-time tests (see Fig. 23).\cite{142,150,151,178}

The observed threshold voltage and mobility shifts induced in flexible IGZO TFTs under tensile/compressive bending have been explained by an increase/decrease of the the carrier density caused either by the creation of oxygen vacancies,\cite{159} or by a change of the electronic structure.\cite{150} These effects (together with the above men-
tioned values) are only valid if the IGZO TFTs are bent within the mechanically elastic region, whereas bending to smaller radii induces cracks that cause permanent parameter shifts or even device failure.\textsuperscript{84,142,151,181} At the same time, it has to be mentioned that other groups also observed no effect or even an opposing influence of mechanical bending.\textsuperscript{148,179,180} These partially contradictory observations (concerning both the direction and the magnitude of strain-induced changes) can be explained by a number of additional factors that need to be considered:

(I) Illumination can have a significant effect on bending measurements. Even if the illumination condition is not reported in the majority of the published bending experiments, it is important to take into account the combined light-strain effect, especially for the fabrication of flexible optical displays. A direct comparison of flexible IGZO TFTs bent while in darkness and under illumination is shown in Fig. 24. Without illumination, the $\mu_{FE}$ and $V_{TH}$ change by 3.1\% (−1.8\%) and −15 mV (19 mV), respectively, under tensile (compressive) strain $\epsilon$ of $\approx \pm 0.3\%$.\textsuperscript{150} Under an illumination of 90 lx, the $\mu_{FE}$ varies by 14.8\% (−3.7\%) and the $V_{TH}$ changes by −110 mV (37 mV) under tensile (compressive) bending.\textsuperscript{150} Additionally, also the relaxation behavior is different: a full recovery of the parameters is possible only if the devices are bent in darkness.\textsuperscript{150} It is important to underline that illumination only influences the magnitude of the measured parameter shifts, whereas the sign depends on the direction of bending (tensile or compressive). Furthermore, a combined effect of mechanical bending, illumination and bias stress on the stability of flexible IGZO TFTs was described by Park \textit{et al.}\textsuperscript{134}

(II) In short-channel TFTs ($L \lesssim 5 \mu m$), the channel resistance ($R_{CH}$) can become comparable to the contact resistance, as well as the resistance of the interconnection lines. Therefore, also the strain sensitivity of the, generally metallic, contacts (and not only of the metal oxide semiconductor) can influence the response of the TFTs under applied mechanical bending.\textsuperscript{113}

(III) Device encapsulation can move the neutral bending axis above the TFT layers, leading to an effective compressive strain induced even if tensile bending is applied.\textsuperscript{139} A similar effect can also occur if the strain built-in in the device layers is larger than the strain induced by bending.\textsuperscript{90,156} In both cases, strain-induced parameter shifts with an opposite algebraic sign are observed.

(IV) The geometry of the TFTs can also influence their strain sensitivity. While BG and TG IGZO TFTs in general exhibit the parameter shifts described above, DG IGZO TFTs show exactly the opposite behavior.\textsuperscript{208} A direct comparison of flexible BG and DG IGZO TFTs bent in tensile direction resulted in a $\mu_{FE}$ and $V_{TH}$ shift of 2\% and −75 mV for BG TFTs, but in shift of −7\% and 25 mV in the DG case, respectively.\textsuperscript{90} Similarly, IGZO VTFTs exhibit $\mu_{FE}$ and $V_{TH}$ shift between −2\% to −5\% and 100 mV to 130 mV while strained by 0.5\%.\textsuperscript{92,144} Here, the Poisson effect leads to the fact that tensile bending results in compressive strain in the device channel.

(V) The influence of repeated bending cycles combined with the specific relaxation behavior causes a time sensitivity of the TFTs during bending experiments. At the same time, different groups also use diverse time scales to apply mechanical bending, with time differences spanning to up to one hour.\textsuperscript{157}
(VI) Furthermore, extensive bending beyond a certain strain value (which delimits the elastic with the inelastic region) can lead to the formation of micro-cracks in different material layers.\textsuperscript{84,142} These cracks can be hardly visible and do not necessarily result in device failure. Nevertheless, TFTs with micro-cracked layers can present different device parts disconnected from each other, and therefore exhibit a reduced $W/L$ ratio, as well as a worst electrostatic control over the channel. In these cases, a decrease of the $I_D$ together with an increase of off current (under both tensile and compressive bending) is observed.

(VII) Finally, the influence of the electrical stress induced by measuring the devices repeatedly during the bending tests needs also to be taken into account. On one hand, it has been reported that the parameter variations caused by mechanical stress (especially cyclic bending) are in the same order of magnitude as the shifts caused by electrical stress (standard gate bias stress measurements).\textsuperscript{150} On the other hand, gate bias stress (positive and negative) induces basically the same shifts, regardless if IGZO TFTs are strained, bent to different tensile radii (down to 40 mm),\textsuperscript{159} or cycled between flat (radius of 15 mm) and bent state for up to 10,000 repetitions.\textsuperscript{154} Also the influence of bending on the AC performance of flexible IGZO TFTs has been analyzed.\textsuperscript{113,114} The AC performance, in particular the $f_T$ is mainly determined by the transconductance $g_m$ and the gate capacitance $C_G$ of the TFTs (see Equation L8). On one side, $g_m$ increases under tensile bending due to the increased $\mu_{FE}$ and decreased $V_{TH}$. On the other side, tensile bending also increases the $C_G$ (typically by 1%-2% for 0.5%-1% tensile strain), due to a increased area, decreased $t_{ox}$, and increased carrier density under bending. Due to the simultaneous increase of $g_m$ and $C_G$, $f_T$ remains basically unchanged.

Additionally, it is also important to predict and simulate the strain sensitivity of TFT (as well as circuits) prior to fabrication, in order to optimize the devices and reduce the strain-induced performance variations as much as possible. One step in this direction was done by Ma et al.,\textsuperscript{216} who included strain-induced $\mu_{FE}$ variations into a HSpice-based flexible circuit analyzer. Furthermore, purely mechanical simulations of flexible n-type vacuum-processed metal oxide semiconductor TFTs have also been done. In particular, COMSOL multi-physics was used to model strain-stress curves, as well as von Mises stress induced by tensile, compressive and torsional forces.\textsuperscript{217} In these mechanical models, IGZO and graphene active layers showed similar performance. Moreover, also device failure due to crack formation was predicted by a finite element method (FEM). The FEM simulations were used for flexible IGZO TFTs to identify device areas prone to stress localization under tensile and compressive bending,\textsuperscript{218} or simulate the strain of a PVP/Al$_2$O$_3$ hybrid gate dielectric.\textsuperscript{151} Finally, the mechanical stress induced in IGZO TFTs roll-transferred onto a flexible PDMS substrate was also calculated by Sharma et al.\textsuperscript{204}

**Improvement of bendability:** As explained above, sub-millimeter bending radii are necessary for many novel applications (e.g. smart textiles, implantable and imperceptible medical devices). While TFTs bending radii of several millimeters or even centimeters can be obtained easily,\textsuperscript{106,133,134,144,146,151,152,154–157,159,160,177,178,203,207} smaller curvatures are more complicated to be achieved.\textsuperscript{22,80,96,139} There are two main approaches to enhance the device bendability: either improving the TFT flexibility, or reducing the mechanical strain induced by bending. In particular, the TFT flexibility can be enhanced in several ways:

(I) The most obvious way is to increase the ductility of the different device layers. An investigation of flexible IGZO TFTs with different metals used as BG (see Fig. 10) showed that the device bendability scales with the ductility of the gate. Flexible IGZO TFTs using Cr (thin film rupture strain $\epsilon_r \approx 0.5\%$), Ti ($\epsilon_r \approx 2\%$), Pt ($\epsilon_r \approx 4\%$), or Cu ($\epsilon_r \approx 4.5\%$) BG exhibit average bendabilities of 4.2 mm, 2.4 mm, 2.2 mm, and 1.9 mm radii, respectively.\textsuperscript{84}

(II) It is also promising to replace the brittle ceramic gate dielectrics (e.g. Al$_2$O$_3$) with more ductile polymers. For example P(VDF-TrFE) can be used without additional insulating layers and results in TFTs with good electrical and mechanical performance.\textsuperscript{148} The use of PVP in combination with 20 nm, 30 nm, or 40 nm thick Al$_2$O$_3$ confirmed that 40 nm thick Al$_2$O$_3$ yields a reduced mechanical stability.\textsuperscript{151} It is also worth mentioning that a comparison of TG TFTs with 25 nm Al$_2$O$_3$ or 100 nm P(VDF-TrFE) in combination with 10 nm Al$_2$O$_3$ resulted in an increase of the minimum bending radius from 4 mm to 4.7 mm.\textsuperscript{145} Therefore, the gain in ductility offered by polymeric dielectrics has to be compared with the increase in thickness and therefore strain (see Equation II.1) of the entire device stack.

(III) Although all the n-type vacuum-processed metal oxide semiconductors employed for flexible TFTs have a similar chemical composition, their mechanical properties can vary significantly. If amorphous IGZO TFTs are compared to nano-crystalline ZnO TFTs (Fig. 25), the flexible IGZO devices exhibit considerably higher bendability ($\approx 5$ mm instead of $\approx 15$ mm).\textsuperscript{182} The worst bendability of ZnO can be explained by its piezoelectric properties, which lead to the creation of an electric field under the applied strain. The so-formed electric field can subsequently influence the TFT performance. Furthermore, the grain boundaries in ZnO can act as nucleation points for micro-cracks.

(IV) Also the source/drain materials can influence the TFT mechanical properties. A study by Chien et al. reported that IGZO TFTs with IZO/Ti source/drain contacts yield better electrical performance and are less sensitive to mechanical bending (down to 3 mm) if compared to devices with only Ti electrodes.\textsuperscript{141}
Figure 25. Evolution of the linear ($\mu_{\text{LIN}}$) and saturation ($\mu_{\text{SAT}}$) mobilities of flexible IGZO and zinc oxide (ZnO) TFTs under tensile bending (reproduced from Cherenack, Münzenrieder, and Tröster with permissions from IEEE). 182

Figure 26. Influence of bending parallel and perpendicular to the channel (and therefore to the current flow) in flexible IGZO TFTs. Parallel bending increases $\mu_{\text{FE}}$ until the TFT is permanently destroyed at $\epsilon \approx 0.7\%$. Perpendicular bending increases $\mu_{\text{FE}}$ for $\epsilon \lesssim 0.3\%$, but results in a strong $\mu_{\text{FE}}$ degradation if the strain is further increased (adapted from Münzenrieder et al. with the permissions from IEEE). 142

(V) The ductility of flexible IGZO TFTs can also be increased by reducing the device area, and thereby the number of micro-cracks induced by repeated cycles of bending and re-flattening cycles. 160

(VI) Another way to increase the TFT ductility can be achieved by aligning the devices relative to the strain. Fig. 26 shows that bending parallel to the IGZO TFT channel increases the carrier mobility until the devices are destroyed above $\epsilon \approx 0.7\%$. 142 Perpendicular bending only slightly increases the $\mu_{\text{FE}}$ for small strain values ($\epsilon \approx 0.3\%$), but leads to a strong $\mu_{\text{FE}}$ degradation if the strain is further increased. The higher sensitivity of TFTs to perpendicular bending (compared to parallel) is caused by a significantly higher cracking probability in this direction (remember that generally $W > L$). 142 This is also confirmed by Hong, Mativenga, and Jang, who reported flexible IGZO TFTs with $L > W$ showing a reduced cracking formation for cyclic bending in the perpendicular direction. 160 A similar experiment performed with ZnO TFTs showed no significant difference for parallel and perpendicular cyclic bending, 178 which can be probably explained by the low strain values always $\leq 0.07\%$.

Alternatively, the strain induced by bending can be reduced using the following techniques:

(I) The strain induced by bending is inversely proportional to the bending radius and approximately proportional to substrate thickness (see Equation II.1). Given the same maximum strain (TFT strain resistance), thinner substrates directly lead to smaller bending radii. Although thin substrates can be difficult to handle and require more complicated fabrication processes, n-type vacuum-processed metal oxide semiconductor TFTs manufactured on a 0.7µm thick hydrogel/PI hybrid substrate, 22 1µm thick parylene, 80,140 5µm thick glass, 178 and 15µm thick PI 160 have been reported. Fig. 27 shows a flexible IGZO TFTs fabricated on a 1µm thick parylene membrane while wrapped around a human hair (radius of 50µm). Due to the thin substrate, the devices are fully operational at 50µm tensile bending radius, which correspond to an induced strain ($\epsilon \approx 0.4\%$). 80

(II) It is also possible to reduce the strain induced in the TFTs by placing the devices in their neutral strain axis thanks to the use of a suitable encapsulation layer. The bending performance of flexible IGZO TFTs fabricated on a 50µm thick PI substrate and encapsulated with
an additional 50µm thick structured PI foil (+5µm epoxy glue) is shown in Fig. 28. By encapsulating the devices, a reduction of the minimum bending radius from ≈4 mm to 0.125 mm was possible.\textsuperscript{139} Additionally, Park et al. fabricated TFTs on 17µm thick polyimide and encapsulated them between layers of PET, which lead to a possible bending radius of 1 mm.\textsuperscript{136} Here, different encapsulation layer thicknesses, cause different distances between the TFTs and neutral strain axis, have been investigated. It was confirmed that TFTs placed on the neutral stain axis exhibit smaller performance parameter shifts that TFTs placed up to 50µm away from the neutral strain axis. The drawback of this method is that the additional encapsulation layer (with similar thickness as substrate) increases also the total stiffness of the final device. At the same time, an encapsulation is anyway necessary in order to increase the robustness of the final device for applications like flexible displays.\textsuperscript{39,40}

**Additional features:** Electrical and mechanical performance are the two most investigated characteristics of flexible n-type vacuum-processed metal oxide semiconductor TFTs. Nevertheless, the unique physical properties of metal oxide semiconductors also enable devices which are transparent, stretchable, dissolvable, mechanically active, and even biomimetic and biodegradable.

**Transparency:** Together with flexibility and stretchability, also transparency is an important requirement to seamlessly embed electronic devices into everyday objects, especially to enable applications such as electronic windshields or smart glasses. To realize transparent devices, metal oxide semiconductor TFTs are ideal candidates, due to the intrinsic transparency of the active layer and of nearly all available gate dielectrics (both metal oxides and polymers). To fabricate an entirely transparent device, also the metallic (and therefore opaque) gate and source/drain contacts have to be replaced by transparent conductors. To manufacture transparent conductors, ITO is the most commonly used material,\textsuperscript{28,78,80,106,134,136,138,154,157,179,187,188,201,203,204} together with IZO,\textsuperscript{132,159,170,183,207} AZO,\textsuperscript{93,133} and In_{2}O_{3}.\textsuperscript{170} Nevertheless, compared to metallic contacts, conductive metal oxide contacts reduce the TFT bendability. An alternative to brittle metal oxide contacts is the use of graphene which combines flexibility, transparency and a high specific conductivity.\textsuperscript{96} For transparent applications, it is essential that not only the device itself but also the substrate is transparent. Unfortunately the most common material (standard PI) is only partially transparent and exhibits a yellowish to brownish color. Nevertheless, a variety of fully transparent substrates compatible with the fabrication of flexible metal oxide semiconductor TFTs are available, including: PET,\textsuperscript{28,69,96,164,170,179,183,187} PEN,\textsuperscript{38,40,41,133,135,138,148,152,157,162,165–167,172,180} PC,\textsuperscript{153,156} transparent PI, and PI-based nano silica composites,\textsuperscript{132,141,143,158} parylene,\textsuperscript{80,140} PDMS,\textsuperscript{78,131,146,204} PVA,\textsuperscript{82} and finally glass and glass-fabric reinforced composites,\textsuperscript{93,159,168,173} The combination of only transparent materials in one device stack results in fully transparent devices.\textsuperscript{78,80,138,187,204} To quantify the transparency of their n-type vacuum-processed metal oxide semiconductor TFTs, some groups also measured the lucency of the devices in the visible wavelength range, reporting average transmittance values between 70 % and 85 %\textsuperscript{132,133,138,159,179,183} for the complete device stack, as well as 80 % (measured on IGZO film only)\textsuperscript{28} or 85 % transmittance of the devices itself in combination with ≈90 % transmittance of the substrate.\textsuperscript{78} The layout and optical performance of IGZO TFTs fabricated on thin flexible glass substrate is illustrated in Fig. 29, where a transmittance value of 80 % was reported.\textsuperscript{159} It is worth mentioning that, if designed and fabricated properly, transparent n-type vacuum-processed metal oxide semiconductor TFTs can also exhibit excellent mechanical properties like bendability down to radii of 50µm,\textsuperscript{80} and stretchability by up to 5 %.\textsuperscript{78}

**Stretchability:** To enable the integration of electronics into soft, stretchable, or even 3D deformed objects, n-type vacuum-processed metal oxide semiconductor TFTs that can not only be bent but also stretched are necessary. Biomedical implants and artificial electronic skin are good examples demonstrating the need for micromechanical devices yielding mechanical properties similar to human skin or other organic tissues. Skin is not only bendable but also stretchable by up to 70 %.\textsuperscript{81} N-type vacuum-processed metal oxide semiconductor TFTs cannot be directly stretched to such a huge value as they can withstand maximum strain values of...
However, recently several approaches have been proposed to realize stretchable n-type vacuum-processed metal oxide semiconductor TFTs with the use of advanced substrates or geometries:

I) First of all, stretchability can be achieved by using composite elastomeric substrates. These composite substrates can be engineered in order to present a globally low elastic modulus, which is locally increased in specifically designated device islands. By limiting the strain in these stiff islands, it is possible to protect the devices from the extensive strain they are subject to during stretching. Nevertheless, it is essential to realize a smooth transition between the areas with high and low stiffness, since abrupt stiffness changes are more prone to stress localization (and therefore also to delamination during stretching). At this aim, Erb et al. used particle reinforcement to increase the stiffness of polyurethane (PU), as well as to realize a smooth transition between stiff and stretchable areas. By adding 20 vol% of magnetically responsive anisotropic alumina microparticles, the stiffness of the PU was increased by 478%. On top of this composite substrate, IGZO TFTs were manufactured. Due to the shadow mask-based fabrication process (PU has only limited resistance against photolithographic chemicals), and the high surface roughness of around 200 nm, the IGZO TFTs yielded only limited device resolution and performance. Furthermore, stretching experiments of the resulting devices were not performed. Another stretchable composite substrate with mechanically graded patches was fabricated by welding layers of PU-based materials with gradually increasing elastic moduli. In this case, the elastic moduli of the layers were adjusted at molecular, nano- and microscale by changing the concentration of the PU hard domains, laponite and alumina platelets, respectively. The resulting elastic moduli spanned from 40 MPa to 5150 MPa. Given the incompatibility also of this substrate with photolithographic chemicals, IGZO TFTs were fabricated on a 1 µm thick polyethylene membrane and afterward transferred to the reinforced islands (Fig. 30a). The IGZO TFTs were fully functional while the substrate was strained by 300% and after 4000 cycles of stretching and relaxation. Fig. 30b shows the evolution of the TFT transfer characteristic under increasing global strain. Moreover, full device operation on the 3D surface of a sphere (R = 14 mm) was demonstrated. In addition to composite PU substrates, recently also engineered elastomeric substrates constituted by PDMS with microfabricated and embedded stiff SU-8 device islands have been reported. The smooth stiff-to-soft transition between SU-8/PDMS and PDMS allows stretching the IGZO TFTs manufactured directly on the device islands of this engineered substrate to 20%. The smooth stiff-to-soft transition between SU-8/PDMS and PDMS allows stretching the IGZO TFTs manufactured directly on the device islands of this engineered substrate to 20%.
100 μm). Using this approach, IGZO TFTs fabricated on a 1 μm thick parylene membrane and then transferred to a pre-stretched elastomer (VHB tape from 3M) were demonstrated. The resulting devices are visualized in Fig. 31a and Fig. 31b, where TFT operation at substrate strain of up to 210% is demonstrated (Fig. 30c). Finally, there is one single report on wrinkled IGZO TFTs directly fabricated on PDMS. In this work, the PDMS was spin coated on a Si wafer and backed at 150°C. Due to the different CTE of the Si wafer and the PDMS, tensile strain was induced into the PDMS. The following TFT fabrication and release of the PDMS resulted in the formation of wrinkles in the interconnection lines, while the epoxy reinforced TFTs stayed flat. These devices showed no significant influence to strain of 5 %, and after more than 100 cycles of compression and stretching, the resulting devices were able to reversibly self-assemble into micro tubes with radii ranging from the millimeter range down to 25 μm. As shown in Fig. 32, the TFTs are not significantly affected by this self actuated deformation.

III) It is also possible to combine wavy geometry and composite substrate. In the works of Park et al. and Sharma et al., ZnO or IGZO TFTs were fabricated on a rigid substrate, covered with an epoxy cap and afterward transferred to a bi-axially pre-stretched PDMS substrate. Release of the pre-formed strain resulted in the formation of wrinkles in the interconnection lines, while the epoxy reinforced TFTs stayed flat. These devices showed no significant influence to strain of 5 %, and after more than 100 cycles of compression and stretching.

**Dissolubility:** Recently, also completely water-soluble metal oxide semiconductor TFTs have been demonstrated. These devices are based on Mo contacts, SiOx gate dielectric, and IGZO semiconductor. The fabrication takes place on a Si wafer coated with a Ni sacrificial layer; subsequently the complete devices are transferred to a water-soluble 20 μm thick PVA substrate. The complete layer stack can be dissolved in 60°C heated de-ionized (DI) water. The PVA substrate for example was completely dissolved after 1800 s.

**Mechanical activity:** Karnaukhenko et al. demonstrated a unique combination of mechanical and electrical performance by fabricating IGZO TFTs on a highly cross-linked hydrogel/PI composite substrate. In this work, the hydrogel acted as a swelling layer, whereas the PI served as a stiff and chemically robust substrate for the TFT fabrication. In response to different chemicals, the resulting devices were able to reversibly self-assemble into micro tubes with radii ranging from the millimeter range down to 25 μm. As shown in Fig. 32, the TFTs are not significantly affected by this self actuated deformation.

### C. Flexible n-type solution-processed TFTs

In this subsection, the materials and fabrication techniques involved in the realization of flexible n-type solution-processed metal oxide semiconductor TFTs will be discussed. Subsequently, the electrical performance and the mechanical properties of the resulting devices will be presented.

**Materials:** As already done for flexible n-type vacuum-processed metal oxide semiconductor TFTs, in the following we will describe the substrates, dielec-
tric layers (barrier, gate dielectric, passivation), and conductive materials (gate, source/drain) employed to manufacture flexible n-type solution-processed metal oxide semiconductor devices.

**Substrates:** Flexible metal oxide semiconductor TFTs fabricated by vacuum- and solution-processed processes share common substrate requirements, such as low surface roughness, flexibility, compatibility with the required process temperatures, as well as resistance against the needed solvents. Compared to vacuum processing of metal oxide semiconductors, solution-deposition techniques typically require higher temperatures (≥250°C). As a result, substrates with high temperature resistance (T_G ≥ 300°C) are necessary. Due to their high T_G ≈ 360°C, PI substrates with thickness ranging from ~3 to 50µm have been widely used.83,144,190,192,196–198,219–222 Polyyarylate (PAR) foils have also been employed,191,199,225,224 given their good temperature stability (T_G ≈ 330°C), combined with a colorless transparency in the visible range. If the semiconductor deposition is performed at lower temperatures (≤150°C), also PES foils (T_G around 200°C) can be utilized.225 In an attempt to reduce the substrate cost, especially when cost-effective high throughput fabrication processes are targeted, also less expensive polymer substrates like PEN189,194–196,226,227 and PET76,193,228,229 have been employed. However, the worse thermal stability of PEN and PET (T_m around 260°C), if compared to PI or PAR, calls for lower process temperatures. Additionally, the use of paper as a substrate material for flexible solution-processed ZnO TFTs has also been investigated.228,230 Finally, flexible glass substrates (100µm) have also been utilized to allow high annealing temperatures (500°C) in solution-processed IGZO TFTs.200

**Barrier layers:** The use of barrier layers for flexible n-type solution-processed metal oxide semiconductor devices has not been widely explored. For example, c-PVP was applied to planarize and smoothen the surface of PES or PI.190,225 Additionally, using PVP on PI foils, Park et al. was able to reduce the substrate surface root mean square (rms) roughness from 3.6 nm down to 0.3 nm.231 Also inorganic barrier layers (e.g. Al_2O_3, SiO_2) have been utilized to planarize, reduce the water permeation, and improve the wettability of PI substrates. Finally, for the purpose of promoting adhesion between PI and either Cr gate contacts or various oxide materials, both SiN_x144 and zirconium oxysulphate have been employed.

**Gate dielectrics:** As for flexible n-type vacuum-processed metal oxide semiconductor TFTs, also in this case metal oxide gate dielectrics grown from vacuum deposition techniques are widely used, especially SiO_2,198,221 and Al_2O_3.144,196 Nevertheless, for solution-deposited metal oxide semiconductors, it is preferable to solution process also the gate dielectric, in order to further benefit from the low-cost large-area approach offered by solution-deposition processes. Within solution-processed gate dielectrics, polymers materials are especially suitable due to the moderate annealing temperatures needed, as well as the high bendability that can be achieved.228 In particular, PMMA and PVA gate dielectrics have been evaluated in combination with flexible solution-processed ZnO, In_2O_3, or IZO TFTs.193,228,232,233 Nevertheless, compared to metal oxide dielectrics, polymers yield a lower ϵ_R and thus result in devices with higher operational voltages. To combine the advantages of metal oxide dielectrics and solution-processing, recently increasingly efforts have been devoted to grow metal oxide dielectrics with low temperature solution-processing techniques. Main breakthrough in this direction has been achieved by Pal et al., who demonstrated the first solution-processed amorphous Al_2O_3 gate dielectric on PI using an annealing temperature of only 200°C.234 Since then, many other groups reported solution-processed Al_2O_3 dielectrics on flexible PI or PAR substrates.191,219,220,223 Zirconium oxide (ZrO_2),190,194,197 and tantalum oxide (Ta_2O_5)200 are other promising metal oxide dielectrics that can be solution-deposited on flexible substrates. In this context, it has been shown that the use of high-ε_R metal oxide dielectrics (e.g. Al_2O_3, ZrO_2, or Ta_2O_5) not only allows lowering the device voltage operation, but also leads to better TFT performance if compared to devices employing dielectrics with lower ε_R (e.g. SiO_2, PMMA, or PVA).83,191,194,199,223 This improvement is generally ascribed to a reduction of the interfacial trap density and thus to an enhancement of the semiconductor-dielectric interface. Another promising class of dielectric materials comprises ionic liquid/gels and polymer electrolytes. As already reported in II B, electrolyte dielectrics allow achieving high C oxide values and therefore low operation voltage typically below ±2 V. Examples of electrolyte gated n-type solution-processed metal oxide semiconductor TFTs were successfully demonstrated on flexible substrates, such as PEN, PI, and paper.189,192,230 Due to the good conformal coating, electrolyte gate dielectrics facilitate also the deposition of structured/rough metal oxide semiconductor, especially nanoparticles (NPs) and nanorods (NRs).

**Contacts:** The contact materials used in n-type solution-processed metal oxide semiconductor TFTs are generally similar to those employed for their vacuum-processed counterparts. source/drain and gate electrodes are mostly made of Al and Au,144,192,230 but also of transparent conducting metal oxides, such as ITO,76,83,189,195,196 IZO,219,220 or zinc indium tin oxide (ZITO).191 In addition to the above mentioned materials, gate contacts are also made of Cr/Al or dual layers of Cr/Au,219,220, which yield a good adhesion. Aiming towards completely solution-processed TFTs, contact materials have also been processed.
via solution-deposition, employing solution-processed PEDOT:PSS gate electrodes\textsuperscript{192} or solution-deposited ITO source/drain and gate contacts.\textsuperscript{83}

**Passivation layers:** The application of passivation layers in flexible n-type solution-processed metal oxide semiconductor TFTs is not very common. The few available examples include Al\textsubscript{2}O\textsubscript{3},\textsuperscript{195,196} and PMMA layers.\textsuperscript{219,220} In particular, 400 nm thick PMMA layers have been utilized to encapsulate flexible solution-processed In\textsubscript{2}O\textsubscript{3} and IGZO TFTs fabricated on thin spin coated PI.\textsuperscript{219,220} Purpose of the PMMA layers was a reduction of the mechanical stress (and therefore crack formation) during the release of the PI foil from the glass carrier.

**Fabrication techniques:** Like for flexible n-type vacuum-processed metal oxide semiconductor TFTs, also solution-processed devices employ similar fabrication techniques (especially for the substrate preparation, layer structuring, and device configuration). Main difference between vacuum and solution-processed TFTs is constituted by the deposition methods, which are focused on solution-processes (for the active layers and sometimes also for the gate dielectrics and contacts).\textsuperscript{87,235,236} After a brief presentation of the substrate preparation methods, the main focus will be on solution-processing techniques (i.e. general remarks, deposition methods, approaches to lower the process temperatures).

**Substrate preparation:** As for vacuum-processed devices, also in this case it is common to employ free-standing polymer foils with thickness \(\geq 50\,\mu\text{m}\).\textsuperscript{144,190,192,196,198,221} Alternatively, polymers can be spin coated onto a carrier substrate (thickness \(\approx 3-18\,\mu\text{m}\)) and subsequently peeled off after the device fabrication has been completed.\textsuperscript{83,219,220}

**General remarks on solution-processing:** Contrary to most organic semiconducting materials, typical metal oxide semiconductors are not at all or only poorly soluble in common solvents. This is why, solution-processing of metal oxide semiconductors cannot occur by simply dissolving the selected materials, but requires a chemical reaction (synthesis) between suitable reagents (the so-called precursors). In general, two approaches can be used to solution-deposit metal oxide semiconducting materials:\textsuperscript{235} (A) The material is first synthesized and tailored into nanoparticles, nanorods, or nanowires.\textsuperscript{76,189,225,226,229,230,237} These nano-scaled shapes are then dispersed in suitable solvents and subsequently deposited and dried. (B) Alternatively, the precursor solution is first deposited and then converted to the final metal oxide semiconducting material, most commonly via thermal annealing at temperatures in the range of 200 to 500 °C, or alternatively via UV irradiation\textsuperscript{87,116,196,199,223,238} The benefit of approach (A) is that the deposition is decoupled from the synthesis, and therefore also from potentially high process temperatures. Using approach (A), crystalline metal oxide semiconductors can thus be easily synthesized and further tailored through their size and shape.\textsuperscript{239} There are, however, a number of drawbacks connected to approach (A). First of all, often a stable dispersion of the materials requires the use of additives or ligands (mainly insulating, which then need to be removed from the final film to improve the contact between particles).\textsuperscript{240} This removal process usually involves thermal annealing above 300 °C, which is in conflict with the use of temperature-sensitive flexible substrates. Alternative, the high-temperature annealing can be substituted by additional low temperature treatments such as UV irradiation, vacuum annealing, or plasma treatments, which anyway complicate the fabrication process.\textsuperscript{194,241,242} Additionally, an active channel layer constituted by nanoparticles inherently features a high number of (grain) boundaries, each one acting as a potential barrier against charge transport. Furthermore, high film porosity and roughness at the interface semiconductor/gate dielectrics have been demonstrated to be detrimental for the TFT performance.\textsuperscript{189,237} The impact of residual ligands, lots of grain boundaries, as well as interfacial roughness generally limit the device mobility of flexible n-type solution-processed metal oxide semiconductor NP TFTs in approach (A) to below \(1\,\text{cm}^2\,\text{V}^{-1}\text{s}^{-1}\).\textsuperscript{189,225,229,230,240} Compared to NPs, NWs with lengths of several micrometer can lead to unhindered transport all over the active channel (even with only a single wire) and consequently result in drastically increased \(\mu\text{FE}\) of over \(120\,\text{cm}^2\,\text{V}^{-1}\text{s}^{-1}\).\textsuperscript{76,226} Nevertheless, difficulties of alignment and accurate placement of the NWs with respect to the source/drain electrodes are a drawback for more widespread applications. In approach (B), the conversion step takes place after the precursor deposition and therefore in direct contact with the substrate material. Depending on the precursor material, temperatures in excess of 300 °C are typically required to achieve a full material conversion, as well as good layer properties.\textsuperscript{243} The commonly high thermal budget required in approach (B) strongly limits the choice of the flexible substrates to materials such as PI\textsuperscript{144,192} or PAR.\textsuperscript{191} Nevertheless, recent efforts have been devoted to the reduction of the annealing temperatures required to solution-process metal oxide semiconductors (and also gate dielectrics)\textsuperscript{37,87,116,236,244} which consequently allows selecting a wider range of substrate materials, including PEN,\textsuperscript{195,196,227} and PET.\textsuperscript{193,228}

**Deposition methods:** As for vacuum-processed devices, also for flexible n-type solution-processed metal oxide semiconductor TFTs, standard vacuum deposition techniques are widely used, especially to manufacture the conductive and dielectric materials. To grow barrier, gate dielectrics and passivation layers, vacuum-deposition
tools like ALD (for Al₂O₃)[83,144,195,196,199] and PECVD (for SiO₂ and SiNx)[76,83,144,198,221] are commonly utilized. For source/drain and gate contact deposition, thermal and e-beam evaporation,

as well as sputtering[76,83,189,191,195,196,219,220] are mainly employed. With regards to solution-deposition processes on flexible substrates, there are several techniques in use. For most of these techniques both approaches (A) and (B) can be employed:

(I) Spin coating is the most common coating method used in research environments[87,236] the film is formed from a liquid precursor ink as a result of the substrate’s rotational motion. The layer thickness can be precisely controlled by parameters like spin speed and duration, as well as precursor concentration. Main advantages of spin coating are process simplicity and low investment costs. Additionally, spin coated films yield homogeneous and reproducible film properties. As a drawback, however, spin coating can only be carried out in batch processes and becomes more challenging when the substrate size is increased. Spin coating technique is commonly utilized for flexible metal oxide semiconductor TFTs to grow In₂O₃[190,196,223], ZnO[194,225,232] and IGZO[83] active layers. Additionally, many dielectrics layers have also been spin coated on flexible substrates, such as organic PVP barrier layers,[190,225,231] or oxide Al₂O₃ and ZrO₂ dielectrics[83,190,191,194,219,220,223].

(II) Drop casting is probably the simplest deposition technique in which a defined volume of solution is manually dispensed at the desired location. To control the drying behaviour of the droplet, the substrate can be kept at elevated temperatures. Subsequent annealing steps can be used to improve the film quality. Especially TFTs based on nanowires,[226] and nanorods,[240] following approach (A) have been demonstrated using this technique.

(III) It is also possible to deposit metal oxide semiconductors on flexible substrates at low temperatures using a simple hydrothermal growth method. Here, the metal oxide formation takes place directly on the substrate surface during the substrate submersion in a heated precursor solution. Growth conditions can be configured to achieve compact films,[193] or NW growth.[245] The deposition time and precursor concentration define the final layer thickness. ZnO TFTs grown at 90 °C on PET substrates were demonstrated by Lee et al. using this method.[193]

(IV) A more sophisticated method is ink-jet printing, which is a digitally controlled drop-on-demand deposition technique. During ink-jet printing, the metal oxide semiconductor is deposited only where needed, preventing thus the waste of material, as well as the need for subsequent patterning steps. As ink-jet patterns can easily be controlled digitally (without the need of a physical mask/template), design alterations and prototyping can be carried out easily. However, due to the patterned deposition, the ink drying conditions need to be specially controlled, in order to avoid irregularities and effects such as the coffee ring formation. Examples of ink-jet printed metal oxide semiconductors include ITO nanoparticles [approach (A)],[246] as well as ZnO, In₂O₃ or ZTO from a precursor solution [approach (B)].[197,238,247]

(V) In the process of spray pyrolysis, a fine spray of the precursor solution is created (using an air-blast or an ultrasonic nozzle) and directed onto a heated substrate.[243] Given a sufficiently high substrate temperature, the precursor immediately undergoes the conversion reaction and forms the final film material. In addition to the specific precursor material and concentration, parameters such as substrate temperature, droplet size and distribution, as well as solvent type and feed rate present the toolbox to fine tune the material parameters. Good film properties of metal oxide semiconductors processed via spray pyrolysis are normally only achieved for temperatures in excess of 300-400 °C[87] thereby ruling out plastic substrates. However, recent advances enabled the realization of spray coated In₂O₃ TFTs at 250 °C[248] on PI substrates.[144] Main advantage of spray pyrolysis is the possibility to automate the spraying process, thus ensuring repeatability of the film characteristics. In addition, the spray pyrolysis deposition could be further up-scaled, and potentially run in a continuous process.

(VI) Aerosol-jet printing combines attributes from spray pyrolysis and ink-jet printing. In aerosol-jet printing, a fine mist is created and then shaped (by an inert carrier gas and a special nozzle design), in order to allow localized and digitally controlled deposition with feature sizes in the order of a few tens of μm (see Fig. 33a). Aerosol-jet printing has recently been utilized to realize the semiconductor (ZnO), dielectric (ionic gel), and the gate electrode (PEDOT:PSS) in flexible TFTs fabricated on PI at temperatures ≤250 °C (see Fig. 33).[192]

(VII) Other solution-processing techniques such as blade/bar coating, slot-die casting, gravure, or flexographic printing are traditionally more in use for organic
lower decomposition temperature of water solvent is attributed to the formation of an [In(OH$_2$)$_6$]$^{3+}$ complex, whose relatively weak coordination bonds can be broken without excessively high annealing temperatures. (II) The combination of precursor and solvent is also important. To allow solution-processing of ZnO active layers at temperatures down to 150 °C, Meyers et al. proposed to form zinc (Zn) ammine complexes in aqueous solution. The precursor preparation was achieved by dissolution of Zn nitrate in water, followed by precipitation of Zn(OH)$_2$ after the addition of NaOH. Several centrifugation and washing steps were applied to remove Na$^+$ and NO$_3^-$ ions in the solution before the final complex was created by addition of aqueous ammonia. This laborious process was simplified by several research groups by directly dissolving ZnO, Zn(OH)$_2$, or ZnO$_2$H$_2$O powder in ammonia solution. In particular, Fleischhaker, Wloka, and Hennig employed a process temperature ≤ 150 °C to fabricate BG ZnO TFTs on flexible PEN substrates with different polymeric dielectrics. Interestingly, Lin et al. combined the Zn ammine approach with a low temperature solution-processable high-$\varepsilon_R$ ZrO$_2$ gate dielectric to realize low-voltage ZnO TFTs fabricated on PEN at a maximum process temperature of 160 °C.

(V) Another effective method to lower the temperatures of solution-processed metal oxide semiconductors is the so-called combustion chemistry approach introduced by Kim et al. The idea behind combustion chemistry is to utilize an exothermic reaction that takes place inside the precursor on the as-deposited film. The locally self-generated energy is then able to further carry on the conversion reaction. In this way, only a small amount of external energy supply (i.e. a low annealing temperature) is required to surmount the energy barrier that activates and carries out the following reaction. The precursor composition was chosen by Kim et al. to include a fuel component, either acetylacetone or urea, as well as metal nitrates (acting as oxidizing agents). Using this technique and limiting the annealing temperature to 200 °C, Kim et al. were able to demonstrate flexible In$_2$O$_3$ devices on PAR substrates.

(VI) Another way to create metal oxide semiconducting materials at low temperatures was proposed also by Kim et al. In their work, Kim et al. employed a mercury lamp with peak performance at 184.9 nm and 253.7 nm...
to photo-activate an UV-absorbing precursor containing In, Ga, and Zn salts under nitrogen environment. The authors described the process as a UV-assisted photo-chemical cleavage of metal alkoxide groups followed by metal-oxide-metal network formation and further densification. An unintentional heating of the substrate to 150°C was demonstrated to be necessary for a successful precursor conversion. The so-formed IGZO films were embedded into TFTs on PAR substrates. Furthermore, similar UV irradiation approaches were used for low temperature solution-processed gate dielectrics (ZrO$_x$ and HfO$_2$). A schematic overview of the UV photoactivation process is shown in Fig. 35.

Finally, it is possible to combine UV illumination and combustion chemistry. In the work by Rim et al., solution-deposited IGZO was formed from a precursor solution containing metal salts (necessary to grow IGZO), as well as additives of acetylacetone and ammonium hydroxide. On one hand, both additives respectively act as fuel and oxidizer component for the combustion reaction. On the other hand, the additives enabled the formation of metal chelate complexes with enhanced UV absorption. Consequently, UV irradiation could be used to initiate the metal oxide semiconductor formation with the support of an exothermic combustion reaction. The authors employed the same processing scheme to solution-deposit ITO and Al$_2$O$_3$ as contact materials and dielectric, respectively.

**Layer structuring:** As for flexible n-type vacuum-processed metal oxide semiconductor TFTs, similar layer structuring methods can be employed for flexible n-type solution-processed metal oxide semiconductor devices. In addition to the standard patterning methods, depending on the specific deposition technique used, additional means to structure the solution-processed layers are possible. Both ink-jet and aerosol jet printing are direct-write methods, meaning the liquid deposition is carried out only where desired. This reduces material waste and avoids further patterning steps. Due to the digital designs and computer controlled deposition, both ink-jet and aerosol printing allow a flexible and fast patterning. Feature sizes from a few tens up to several hundreds of microns can be easily achieved with these techniques. Although not inherently a direct-write method, spray pyrolysis can be combined with shadow masking, as demonstrated for flexible In$_2$O$_3$ TFTs on PI. This technique, however, so far is limited to line widths above ≈ 100 µm. The specific process of combining UV illumination and combustion chemistry shown by Rim et al., renders irradiated areas insoluble. In this way, UV treatment through a shadow mask can be used to photo-pattern the layers with line widths down to 3 µm. This deposition and patterning method (so-called direct light pattern integration) was employed for IGZO, ITO and Al$_2$O$_3$ layers. Recently, promising results of the first roll-to-roll compatible fabrication of In$_2$O$_3$ patterns on PI substrates via flexographic printing were also demonstrated.

**Device configuration:** The majority of the reported flexible n-type solution-processed metal oxide semiconductor TFTs are fabricated in BG staggered configuration with only few devices in BG coplanar, TG staggered, or TG coplanar setup. Only electrolyte gated devices present a configuration where source/drain and gate electrodes are all in the same plane (in-plane configuration).

**Electrical properties:** Flexible solution-processed TFTs based on n-type metal oxide semiconductors show a broad range of electrical performance parameters, depending on the materials, the deposition approach and technique, as well as the maximum process temperature. An overview of the performance parameters extracted from recently demonstrated flexible n-type solution-processed metal oxide semiconductor TFTs is presented in Table III. First of all, the performance strongly depends on the solution-deposition approach: (A) nano-scaled shapes or (B) precursor-based. As regards devices based on approach (A), a wide range of performance parameters can be obtained in dependence of the employed shape (NPs, NRs or NWs). On one hand, flexible NP TFTs typically yield a low $\mu_{FE} \lesssim 1 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$, The limited performance of flexible NP-based devices can be attributed to the large surface roughness of flexible foils (if compared to rigid Si or glass substrates), which challenges the realization of high-quality nanoparticles. On the other hand, NWs allow realizing longer TFT channels (extending over several microns) based on long range and undisturbed crystalline metal oxide semiconductors. Therefore flexible NW metal oxide semiconductor devices exhibit higher $\mu_{FE}$ up to 120 cm$^2$V$^{-1}$s$^{-1}$ (for In$_2$O$_3$ NW TFTs on PET) if compared to NP TFTs. Nevertheless, the random orientation and placement of NWs currently
This group includes devices with categories, according to their performance:

- Precursors \[\text{Approach (B)}\] are preferable. Flexible TFT hinders their integration in large-area substrates. Especially for integration purposes, TFTs based on n-type metal oxide semiconductor solution-processed from precursors [Approach (B)] are preferable. Flexible TFT based on metal oxide semiconductor solution-processed from precursors can be roughly sorted into three main categories, according to their performance:

(1) This group includes devices with \(\mu_{FE} \leq 1 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\). For example, Bubel and Schmechel used a mechanical layer compaction technique to increase the carrier mobility of ZnO NP-based TFTs from originally \(5 \times 10^{-5}\) to about \(7 \times 10^{-3}\). Another possible approach consists in removing the ligand layer of the nanoparticle film via plasma treatment, or UV irradiation. Lin et al. used room-temperature UV treatment to convert formerly unresponsive nanoparticle films into functional active layers, resulting in TFTs with a \(\mu_{FE}\) of \(\approx 10^{-3}\). However, a higher process temperature is only beneficial within a given material system and TFT configuration. In some cases, the choice of the semiconductor composition and of the gate dielectric is more important. For example, TFTs based on Ga-doped In\(_2\)O\(_3\) annealed at 300 \(^\circ\)C and \(n\)-type In\(_2\)O\(_3\) gate diode exhibited \(\mu_{FE} = 0.4 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\), whereas devices with In\(_2\)O\(_3\) annealed at only 150 \(^\circ\)C and \(n\)-type In\(_2\)O\(_3\) gate diode yielded \(\mu_{FE} = 7.7 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\). Combining low temperature solution-processed Al\(_2\)O\(_3\) and combustion synthesized In\(_2\)O\(_3\) at a maximum temperature of 225 \(^\circ\)C, Yu et al. demonstrated neat crystalline In\(_2\)O\(_3\) TFTs on PAR with a \(\mu_{FE}\) as high as 22 cm\(^2\)V\(^{-1}\)s\(^{-1}\). Another interesting approach to realize low temperature high-performance devices was recently reported by Lin et al. In the work by Lin et al., instead of relying on the bulk mobility of a specific semiconductor, multiple ultra-thin (\(\leq 10\) nm) layers of individual metal oxide semiconductors (either In\(_2\)O\(_3\), Ga\(_2\)O\(_3\), or ZnO) were deposited in different stacking sequences to form quasi-superlattice structures. The best results were obtained using a solution-processed high-\(\varepsilon_R\) ZrO\(_2\) gate dielectric with an active layer sequence of In\(_2\)O\(_3\)/Ga\(_2\)O\(_3\)/ZnO/Ga\(_2\)O\(_3\)/In\(_2\)O\(_3\). Using this approach and a maximum process temperature of 175 \(^\circ\)C, flexible TFTs with a \(\mu_{FE}\) of 11 cm\(^2\)\text{V}^{-1}\text{s}^{-1}\) could


<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>Maximum Temperature (°C)</th>
<th>Mobility (cm(^2)\text{V}^{-1}\text{s}^{-1})</th>
<th>Threshold Voltage (V)</th>
<th>Current On/Off Ratio</th>
<th>Substrate Thickness (µm)</th>
<th>Bending Radius (mm)</th>
<th>Strain (%)</th>
<th>Bending Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZnO NR TFT with ion-gel electrolyte gate dielectric (^{230})</td>
<td>Drop-casting</td>
<td>150</td>
<td>0.03</td>
<td>0.8</td>
<td>10(^2)</td>
<td>1.1</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>In(_2)O(_3) NP TFT with electrolyte gate dielectric (^{139})</td>
<td>Ink-jet printing</td>
<td>RT</td>
<td>0.8</td>
<td>0.55</td>
<td>2 \times 10(^3)</td>
<td>125</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>ZnO TFT with PPy gate dielectric (^{246})</td>
<td>Spin coating</td>
<td>200</td>
<td>0.09</td>
<td>5.4</td>
<td>10(^5)</td>
<td>12</td>
<td>4.3</td>
<td>-</td>
</tr>
<tr>
<td>ZnO TFTs with ion-gel electrolyte gate dielectric (^{192})</td>
<td>Aerosol-jet printing</td>
<td>250</td>
<td>1.6</td>
<td>0.97</td>
<td>10(^5)</td>
<td>50</td>
<td>25</td>
<td>1</td>
</tr>
<tr>
<td>Quasi-superlattice metal oxide semiconductor TFTs with ZrO(_2)/Al(_2)O(_3) gate dielectric (^{27})</td>
<td>Spin coating</td>
<td>175</td>
<td>11</td>
<td>0.5</td>
<td>10(^5)</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>In(_2)O(_3) TFTs (^{144})</td>
<td>Spray pyrolysis</td>
<td>250</td>
<td>0.2</td>
<td>5.29</td>
<td>6 \times 10(^3)</td>
<td>50</td>
<td>4</td>
<td>0.65</td>
</tr>
<tr>
<td>IGZO TFTs with Al(_2)O(_3)/ZrO(_2) gate dielectric (^{233})</td>
<td>Spin coating</td>
<td>150</td>
<td>7.7</td>
<td>1.26</td>
<td>10(^9)</td>
<td>3</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>IGZO TFTs (^{83})</td>
<td>Spin coating</td>
<td>350</td>
<td>84</td>
<td>0.6</td>
<td>10(^3)</td>
<td>18</td>
<td>10</td>
<td>-</td>
</tr>
</tbody>
</table>

Table III. Set of performance parameters extracted from recently demonstrated flexible n-type solution-processed metal oxide semiconductor TFTs, together with fabrication details (i.e. maximum process temperature and semiconductor deposition technique).
be realized on PEN substrates. It was found that the high $\mu_{FE}$ obtained is a result of electron confinement at the metal oxide semiconductor hetero-interfaces of the low-dimensional films. The direct light pattern (DLP) integration process proposed by Rim et al. has also been demonstrated to be successful to realize low temperature high-performance flexible devices.\(^{83}\)

Using DLP and a process temperature of 350°C, fully transparent and solution-processed TFTs with IGZO semiconductor, ITO contacts and Al$_2$O$_3$ gate dielectric yielding a remarkably high $\mu_{FE}$ of 84 cm$^2$/V·s\(^{-1}\) were fabricated (Fig.36). In a study by Dai et al. another means for device improvement was demonstrated by blending IGZO precursors with graphene nanosheets.\(^{200}\)

The graphene acts as a conductive filler that assists charge transport in the IGZO films and increases $I_{ON}$. However, by keeping graphene concentrations below the percolation threshold, the drain currents of TFTs in the off-state remained low, thus increasing the overall device performance. Albeit at high process temperatures of 550°C, using a high-$\epsilon_R$ Ta$_2$O$_5$ gate dielectric and a thin, thermally stable glass substrate, bendable low-voltage IGZO/graphene TFTs with $\mu_{FE} = 73.6$ cm$^2$/V·s\(^{-1}\) were realized.

**Mechanical properties:** Given the recent advances in low temperature solution-processing of metal oxide semiconductors, an increasing number of works on flexible n-type solution-processed TFTs has been published. However, as the field is still rather premature, often mechanical bending tests are not reported.\(^{76,189,190,193–196,199,223,227,232}\)

Nevertheless, some groups have presented single bending tests (tensile and compressive) at radii between 25 and 1 mm, as well as cyclic bending up to 10 000 cycles.\(^{83,144,191,192,198,200,219–221,224,225,228,239,231}\)

In the case of flexible TFTs with nano-scale shapes, it has been demonstrated that the application of mechanical bending causes a deformation of the particle network. In particular, tensile strain slightly increases the distance between individual particles, resulting in a lower $\mu_{FE}$.\(^{225}\) For example, tensile bending at a radius $R \leq 8.5$ mm leads to crack formation and early device failure in ZnO NR TFTs, whereas the same devices are fully operational down to compressive bending radius of 1.1 mm.\(^{230}\)

In flexible TFTs with precursor-based solution-processed semiconductors, strain-induced device failure is mainly attributed to the formation of cracks or voids in the less ductile device layers. Device failure is often caused by strain-induced breakdown in the gate dielectric layers, e.g. in SiO$_2$ in combination with amorphous In$_2$O$_3$:Ga\(^{198}\) or thin ZnO (8 nm)\(^{221}\) metal oxide semiconductor. While solution-processed Al$_2$O$_3$ layers can withstand up to 320 bending cycles without failure,\(^{83,191}\) polymeric (PVP),\(^{228}\) polymer-oxide hybrids (PVP with 15 nm ZrO$_2$)\(^{231}\) or electrolyte\(^{192}\) gate dielectrics are fully functional up to 10 000 repetitions. The contacts can also originate device failure, especially in the case of brittle ITO electrodes. For example, Song et al. attributed the failure of ZnO TFTs (50μm PI/50 nm ITO/270 μm SiO$_2$/8 nm ZnO/50 μm Al) during real time bending tests (e.g. manual crumpling of the devices) to the formation of fractures in either the electrodes or the dielectric.\(^{221}\)

Device degradation in the active layer is mostly attributed to the use of crystalline metal oxide semiconductors,\(^{191,231}\) or to a high number of bending cycles paired with a small bending radius.\(^{192}\)

The difference between amorphous and crystalline metal oxide semiconductors is illustrated in a study by Yu et al., where crystalline In$_2$O$_3$ and amorphous In$_2$O$_3$-PVP were compared (see Fig.37).\(^{191}\)

The PVP-In$_2$O$_3$ devices resulted in improved mechanical properties at 10 mm radius: $\mu_{FE}$ reduced to only ≈18% instead of the ≈98% decrease reported for crystalline TFTs. The difference in behavior was related to crack formation within the neat In$_2$O$_3$, whereas the doped layers remained crack free. Additionally, in another work it was shown that blending an IGZO precursor with graphene nanosheets allows improving the resistance to bending stress.\(^{200}\)

While TFTs with neat IGZO results in a mobility degradation of 70% over 100 bending cycles, the IGZO/graphene device only varies by 8%.

**Transparency:** Due to the wide band gap ($E_g$) of metal oxide semiconductors, the realization of flexible and transparent n-type solution-processed devices is established. Aside from PI, all the other common plastic substrate materials, metal oxide semiconductors, and also most of the gate dielectrics are transparent in the visible range. To fabricate fully transparent flexible TFTs, ITO or IZO electrodes need to be used.\(^{195,196}\)

Visible light transmittance of entire device stacks yield values between 76 and 81% for In$_2$O$_3$-PVP blends on PAR,\(^{191}\) and In$_2$O$_3$ NW on PET substrate,\(^{28}\) respectively.
III. P-TYPE OXIDE SEMICONDUCTOR TFTS

To complete the analysis of flexible oxide semiconductor TFTs started in section II, here we will present the ongoing research on flexible p-type devices based on oxide semiconductors. First, in III A, the available p-type oxide semiconductor materials will be presented. Next, in III B and III C the state-of-the-art flexible p-type TFTs based on vacuum- and solution-processed oxide semiconductors are shown. To complete the analysis of flexible metal oxide semiconductor TFTs started in section II, in this section we will present the ongoing research on flexible p-type devices based on metal oxide semiconductors. First, in III A, the available p-type metal oxide semiconducting materials will be presented. Next, in III B and III C the state-of-the-art flexible p-type TFTs based on vacuum- and solution-processed metal oxide semiconductors are shown.

A. P-type metal oxide semiconductors

In general, p-type metal oxide semiconductors are characterized by a band gap $E_g$ ranging from 1.3 eV to 2.7 eV,\textsuperscript{71,74} high transmittance in the visible range (> 85%),\textsuperscript{256,257} and carrier density (N) from 10\textsuperscript{8} cm\textsuperscript{-3} (for NWs),\textsuperscript{258} to 10\textsuperscript{15} cm\textsuperscript{-3} (for high-quality single crystals).\textsuperscript{73} Already since 2005 when the first p-type TFT based on Zn-doped Ga\textsubscript{2}O\textsubscript{3} (Ga\textsubscript{2}O\textsubscript{3}:Zn) NWs was realized by Chang et al.,\textsuperscript{76} it was clear that the main limitation of p-type metal oxide semiconductors was linked to their electronic structure.\textsuperscript{71} As already explained in II A, the majority of metal oxide semiconductors are characterized by CBM with spatially spread metal orbitals (s) and VBM with rather localized oxygen orbitals (2p).\textsuperscript{71} Such an electronic structure guarantees a good electron conduction (and therefore a large electron mobility), and at the same time a bad hole transporting path (low hole mobility due to hopping conduction).\textsuperscript{71}

To date, only a few metal oxide semiconductors (e.g. SnO\textsubscript{2},\textsuperscript{71,72,79,256,257,259–278} and Cu\textsubscript{2}O\textsuperscript{73,74,266,279–293}) present a slightly different electronic structure. In particular, SnO\textsubscript{2} is an interesting p-type semiconductor, because its VBM is formed by hybridized orbitals of localized oxygen (2p) and spatially spread Sn metal (5s).\textsuperscript{72} SnO\textsubscript{2}-based TFTs were first introduced in 2008-2009 by Ogo et al.,\textsuperscript{71,72} with a $\mu_{FE} = 1.3 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and an $I_{ON}/I_{OFF} \approx 10^2$ (at a process temperature of 575°C). Following extensive improvements of the deposition techniques combined with deep material analysis,\textsuperscript{256,257,259,277,279} SnO\textsubscript{2} devices with $\mu_{FE}$ ranging from 1 to 10 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1} can now be reliably realized at process temperatures $\leq$ 300°C.\textsuperscript{256,270–272,275,277,278} Also Cu\textsubscript{2}O has an interesting electronic structure, with a VBM composed by hybridized orbitals of O\textsubscript{2} (2p) and Cu metal (3d).\textsuperscript{281} First p-type Cu\textsubscript{2}O TFTs were demonstrated by Matsuzaki et al. in 2008 with a $\mu_{FE} = 0.26 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and an $I_{ON}/I_{OFF} \approx 6$ (at a process temperature above 650°C).\textsuperscript{73} Nowadays, p-type Cu\textsubscript{2}O TFTs with a $\mu_{FE}$ up to 4.3 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1}\textsuperscript{283} can be manufactured at process temperatures ranging from RT to 500°C.\textsuperscript{281,283,288,290} Interestingly, p-type TFTs based on bi-layers of SnO and Cu\textsubscript{2}O have also been shown.\textsuperscript{295} Additionally, devices based on solution-processed SnO\textsubscript{2} and Cu\textsubscript{2}O\textsubscript{290,292,296} have also been presented. Besides SnO\textsubscript{2} and Cu\textsubscript{2}O, also NiO has been utilized to realize rigid p-type TFTs with modest carrier mobility.\textsuperscript{75,297,298} Moreover, doping of n-type metal oxide semiconductors has also enabled the demonstration of p-type TFTs, such as rigid NW devices based on P- and N-doped ZnO,\textsuperscript{258,299} as well as the already reported Ga\textsubscript{2}O\textsubscript{3}:Zn.\textsuperscript{70} Among all the reported p-type metal oxide semiconductor TFTs,\textsuperscript{70–75,79,256,277,279–293,299} only few devices have been fabricated on flexible substrates.\textsuperscript{35,79,256,266,271,272,284,288} This is mainly due to the high deposition and annealing temperatures (typically $\geq 200$°C) that are required, which are mostly incompatible with flexible temperature-sensitive substrates. This is why alternative p-type active layers that allow RT processing are under investigation. An interesting p-type semiconducting inorganic molecular compound is copper (I) thiocyanate (CuSCN), which is characterized by wide $E_g$ (3.7 - 3.9 eV) and high optical transparency.\textsuperscript{300} The first CuSCN devices presented by Chen and Könenkamp in 2003 were based on a flexible NW TFT geometry.\textsuperscript{301} Subsequently, TFTs with spin coated CuSCN layers have been demonstrated on both glass and Si substrates ($\mu_{FE} = 0.5 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$).\textsuperscript{300,302} Further details about the progress of p-type oxide semiconductors on rigid substrates have been reported in other reviews.\textsuperscript{119}

Metal oxide semiconductors for flexible TFTs

Not all of the above mentioned metal oxide semiconductor materials have been employed as active layers in flexible TFTs.

Vacuum-processed metal oxide semiconductors

For flexible devices, only SnO\textsubscript{2},\textsuperscript{79,256,266,271,272} and
Cu$_2$O$^{284,288}$ active layers have been employed. Flexible SnO$_2$ TFTs exhibit $\mu_{FE}$ up to 5.87 cm$^2$ V$^{-1}$ s$^{-1}$, whereas Cu$_2$O TFTs yield lower performance ($\mu_{FE} \leq 0.0022$ cm$^2$ V$^{-1}$ s$^{-1}$).$^{284}$

Solution-processed metal oxide semiconductors Even if solution-processed p-type SnO$_2$,$^{267}$ Cu$_2$O,$^{290,292,296}$ and NiO$^{297}$ TFTs have been fabricated on rigid substrates, there is no report on flexible p-type solution-processed metal oxide semiconductor devices. As already mentioned above, CuSCN offers a valid inorganic alternative and can be easily deposited by spin-coating.$^{300,302}$ In III C, we will present unpublished results on flexible p-type TFTs based on spin coated CuSCN films.

B. Flexible p-type vacuum-processed TFTs

In this subsection, the materials and fabrication techniques involved in the fabrication of flexible p-type vacuum-processed metal oxide semiconductor TFTs will be discussed. Subsequently, the electrical performance and the mechanical properties of the resulting devices will be presented.

Materials: In the following, we will describe the substrates, dielectric layers (barrier, gate dielectric), and conductive materials (gate, source/drain) employed to fabricate flexible p-type vacuum-processed metal oxide semiconductor TFTs.

Substrates: Also in this case, the substrates need to fulfill several requirements, such as compatibility with the fabrication process (high $T_G$ and $T_m$, reduced outgassing, chemical stability), good mechanical properties, sometimes even combined with specific features, such as high transparency, bio-compatibility and lightness. Also for flexible p-type vacuum-processed metal oxide semiconductor TFTs, there are two different approaches: in the first one, the substrate is not part of the device and is only used as a mechanical support.$^{284,288}$ In this case, well known materials, such as PI,$^{256,272}$ PET,$^{288}$ and PES$^{284}$ are used. In the second approach, similarly to Si technology, the substrate is a layer of the device itself. As shown in Fig.38, cellulose fiber-based paper (thickness $\approx$ 75$\mu$m) is used as both substrate and gate dielectric.$^{79,266,271}$

Barrier layers: In this case the use of barrier layers to encapsulate and electrically insulate to substrate is rare. Indeed, only Caraveo-Frescas, Khan, and Alshareef presented a PI substrate covered by 200 nm Si$_3$N$_4$.$^{272}$

Gate dielectrics: The most common gate dielectrics are HfO$_2$,$^{256}$ Al$_2$O$_3$,$^{284}$ AlN,$^{288}$ ferroelectric P(VDF-TrFE)$^{272}$ as well as cellulose fiber-based paper.$^{79,266,271}$

Contacts: As already explained in II, the gate contact is mainly chosen based on a high compatibility with the fabrication process, while the source/drain electrodes need to provide also high conductivity and small $R_C$ with the active layer. For the gate contact, Al$^{272}$ as well as multi-layer metals (like Ni/Au/NI$^{284}$) and transparent compounds (ITO$^{256,288}$ and IZO$^{79,266,271}$) have been used. At the same time, for source/drain metals, single (Al$^{266}$ and Au$^{288}$) and multi-layer contacts (Ti/ITO$^{256}$, Ti/Au$^{272}$ and Ni/Au$^{79,271,284}$) were chosen.

Fabrication techniques: Like flexible n-type vacuum-processed metal oxide semiconductor TFTs, also their p-type counterparts employ similar fabrication techniques.

Substrate preparation: The most common substrate preparation approach is to use free-standing flexible substrates.$^{79,256,266,271,272,284,288}$

Deposition methods: The main deposition technique employed for p-type vacuum-processed metal oxide semiconductors is sputtering. SnO$_2$ and Cu$_2$O are deposited by both DC$^{256,272,288}$ and RF sputtering$^{79,266,271,284}$ One of the main concerns to ensure full compatibility of p-type metal oxide semiconductors with flexible substrates is the post-deposition annealing temperature, that needs to be kept typically below 160°C. As shown in Table IV, there is only one report where the annealing is performed at room-temperature,$^{288}$ whereas all other devices require higher temperatures.$^{35,79,256,266,271,272,284}$ The deposition of gate dielectrics has been performed using ALD$^{256,284}$ magnetron sputtering$^{288}$ or spin-coating.$^{272}$ For the metal contacts, the main deposition techniques are e-beam evaporation,$^{79,256,271,284}$ thermal evaporation,$^{272}$ and sputtering.$^{256}$ The only barrier layer reported (Si$_3$N$_4$) has been grown by PECVD.$^{272}$

Layer structuring: The patterning of the different device layers is strictly related to the substrate nature. In case of large feature sizes and chemically unstable substrates, shadow masking is used.$^{79,271,284}$ For chemically stable substrates (e.g. PI and PET), UV
photolithography is chosen.  

**Device configuration:** Two main device configurations have been employed for flexible p-type vacuum-processed metal oxide semiconductor TFTs:

(I) Due to an easier processing, BG structures are very common. For both coplanar and staggered configurations, the passivation layer is always omitted.

(II) TG (typically coplanar) TFTs are used when fragile layers such as PVDF-TrFE are implemented in the device structure, with the advantage of having an already passivated active layer.

**Electrical properties:** The research in the field of p-type metal oxide semiconductor TFTs aims at reaching similar device performance levels as their n-type counterparts. Table IV compares the performance obtained for state-of-the-art flexible p-type vacuum-processed metal oxide semiconductor TFTs. The DC performance include $\mu_{FE}$ up to 5.87 cm$^2$ V$^{-1}$ s$^{-1}$ demonstrated for fully transparent SnO TFTs on PI (Fig.39). Such record $\mu_{FE}$ (at a low process temperature of 180 °C) has been possible by carefully engineering the SnO phase. In particular, a well-controlled amount of Sn residuals was employed. The threshold voltage and the on/off current ratio range from $-11.73$ V to $1.4$ V, and from $100$ to $4 \times 10^4$, respectively. To date, no AC performance of flexible p-type vacuum-processed metal oxide semiconductor TFTs has been reported.

**Mechanical properties:** Given the small number of publications on flexible p-type vacuum-processed metal oxide semiconductor devices, there is only one report on TFT mechanical bendability. In particular, only Caraveo-Frescas, Khan, and Alshareef showed flexible SnO ferroelectric devices bent for 200 cycles at a bending radius of 10 mm yielding a $\mu_{FE}$ decrease of about 20% (see Fig.40).

**C. Flexible p-type solution-processed TFTs**

As already explained in III.A and III.B, the field of flexible p-type metal oxide semiconductor TFTs is pretty unexplored, and there are still many challenges to be solved. No wonder that to date, there is no report on flexible p-type solution-processed metal oxide semiconductor TFTs. As already mentioned, CuSCN represents a valid inorganic alternative to p-type metal oxide semiconductors (especially if solution-deposited). In this subsection, we will present some preliminary results we recently achieved with flexible p-type TFTs based on spin-coated CuSCN films.

**Materials and fabrication techniques:** Flexible BG coplanar and TG staggered CuSCN TFTs have been fabricated on 50 μm free-standing PI foils. Prior to the TFT fabrication, 50 nm SiNx adhesion and barrier layers were deposited by PECVD on both sides of the substrate. Two different gate dielectrics were employed: for the BG devices $A_2O_3$ (25 nm) grown by ALD, and for the TG TFTs spin-coated 160 nm-thick poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) [P(VDF-TrFE-CFE)]. In particular, P(VDF-TrFE-CFE) is a high-$\epsilon_R$ relaxor ferroelectric polymeric dielectric that can be easily solution-processed at low temperatures. For the solution-processed gate dielectric preparation,
the P(VDF-TrFE-CFE) at 56/36.5/7.5 mol% was first synthesized and then dissolved in methyl-ethyl-ketone (MEK). As spin coated P(VDF-TrFE-CFE) films were subsequently annealed at 60 °C. For both BG and TG TFTs, the active layer solution was prepared by dissolving the CuSCN precursor in dipropylsulfide. The resulting solution was then stirred, centrifugated, filtered, spin coated at room-temperature and annealed at 80 °C, resulting in a 15nm thick CuSCN film. The gate electrodes were formed by evaporated Cr (for the BG TFT) and Al (for the TG TFT), whereas the source/drain contacts were made of evaporated Ti/Au (for the BG) and Au (for the TG). BG TFTs were left unpassivated, while TG devices were intrinsically passivated by the P(VDF-TrFE-CFE) gate dielectric. For the CuSCN BG TFTs, the structuring of all layers (except for the unpatterned SiN and CuSCN) was performed by standard UV photolithography. In the case of the TG devices, layer patterning of the gate and source/drain electrodes was performed by shadow masking, whereas the P(VDF-TrFE-CFE) gate dielectric was left unstructured.

Electrical properties: The flexible CuSCN BG TFTs with Al2O3 gate dielectric yield a $\mu_{FE} = 0.0013 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, a $V_{TH} = -1 \text{V}$, and an $I_{ON}/I_{OFF} = 5 \times 10^2$. The flexible CuSCN TG devices with solution-deposited P(VDF-TrFE-CFE) gate dielectric exhibit a $\mu_{FE} = 0.0012 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, $V_{TH} = -3 \text{V}$, and $I_{ON}/I_{OFF} = 2 \times 10^3$, combined with a small gate-induced hysteresis (as visible from Fig. 41). Due to the high-$\epsilon_R$ gate dielectrics, both BG and TG devices can be operated at low $V_{GS}$ and $V_{DS}$, up to -3.5 V and -10 V, respectively. Even if the achieved carrier mobility is lower than the values presented for rigid devices, these preliminary results are very promising especially in view of future process and device optimization.

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Deposition Method</th>
<th>Deposition Temperature (°C)</th>
<th>Mobility (cm² V⁻¹ s⁻¹)</th>
<th>Threshold Voltage (V)</th>
<th>Current On/Off Ratio</th>
<th>Substrate Thickness (μm)</th>
<th>Bending Radius (mm)</th>
<th>Bending Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu2O TFT with Al2O3 gate dielectric</td>
<td>RF Sputtering</td>
<td>Room/150</td>
<td>0.0022</td>
<td>-4.75</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SnO2 TFT with and on paper (substrate and gate dielectric)</td>
<td>RF Sputtering</td>
<td>Room/150</td>
<td>1.3</td>
<td>-1.4</td>
<td>$10^2$</td>
<td>75</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SnO2 TFT with and on paper (substrate and gate dielectric)</td>
<td>RF Sputtering</td>
<td>Room/160</td>
<td>1.2</td>
<td>-</td>
<td>$10^2$</td>
<td>75</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Nano-crystalline Cu2O TFT with AlN gate dielectric on PI</td>
<td>DC Sputtering</td>
<td>Room/</td>
<td>0.8</td>
<td>-</td>
<td>$4 \times 10^3$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SnO2 TFT with and on paper (substrate and gate dielectric)</td>
<td>RF Sputtering</td>
<td>Room/160</td>
<td>1.3</td>
<td>1.4</td>
<td>$10^2$</td>
<td>60</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SnO TFT with HfO2 gate dielectric on PI</td>
<td>DC Sputtering</td>
<td>Room/150</td>
<td>5.87</td>
<td>-</td>
<td>$6 \times 10^3$</td>
<td>-</td>
<td>10</td>
<td>200</td>
</tr>
<tr>
<td>SnO TFT with ferroelectric P(VDF-TrFE-CFE) gate dielectric on PI</td>
<td>DC Sputtering</td>
<td>Room/200</td>
<td>2.51</td>
<td>-11.73</td>
<td>$10^2$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Table IV. Performance parameters extracted from recently demonstrated flexible p-type vacuum-processed metal oxide semiconductor TFTs, together with fabrication details (i.e. semiconductor deposition technique, deposition/annealing temperature).

Figure 41. Transfer characteristics of a flexible solution-processed CuSCN TFT with Poly(vinylidene fluoride-trifluorooethylene-chlorofluorooethylene) [P(VDF-TrFE-CFE)] gate dielectric, measured while the device is flat and bent to 5 mm tensile bending radius. The inset shows a photograph of the flexible TFT characterized while being bent.

Mechanical properties: Both BG and TG CuSCN devices are also fully operational when mechanically bent down to 5 mm tensile radius, and show only small strain-induced shifts (displayed in Fig. 41 for a flexible TG device). In particular, the $V_{TH}$ changes by only -10 mV and -30 mV for BG and TG, respectively. In BG and TG devices, the hole mobility is reduced by 23% and 16%, respectively.

IV. METAL OXIDE SEMICONDUCTOR-BASED CIRCUITS

In this section, metal oxide semiconductor-based electronic circuits are introduced. In IV A, an overview on basic analog and digital circuit configurations and operation is given. Next, in IV B state-of-the-art electronic circuits based on unipolar metal oxide semiconductors are reported. Finally, in IV C complementary circuits based
on hybrid organic/metal oxide semiconductors, as well as only on metal oxide semiconductors are presented.

A. Circuit configuration and operation

In this subsection, the most common circuit configurations will be presented, followed by an explanation of digital and analog circuit basic operation.

Circuit configuration: As already explained, n-type metal oxide semiconductor TFTs, compared to p-type metal oxide semiconductor devices, yield a better performance, and can be also easier deposited at low process temperatures. This is why the majority of flexible (and also rigid) metal oxide semiconductor-based circuits are unipolar operating with only n-type TFTs, whereas flexible complementary circuits based on both n- and p-type devices are rare. Such disparity between n- and p-type devices renews an old challenge encountered in Si technology back in the 1970’s and 1980’s when the circuits where built using only one semiconductor polarity (NMOS or PMOS logic). Fig. 42 displays the two main configurations using n-type TFTs (shown in the case of a logic inverter): a) the first one is unipolar with only an n-type device and a resistive pull-up load, whereas b) the second one is complementary with both n- and p-type devices. The main difference between the two setups occurs when a digital high level (‘1’) is applied at the inverter input (IN) and the n-type TFT is turned on. In this situation, there is always a current flowing through the supply voltage ($V_{DD}$) and the ground (GND) of the unipolar circuit (Fig. 42a), whereas there is no DC current flow in the complementary inverter (Fig. 42b) due to the switched off p-type TFT. The absence of a DC current for a high digital input in the complementary circuit allows achieving higher gains and lower DC power consumption. For flexible metal oxide semiconductor-based circuits, also other unipolar (NMOS) pull-up implementations are employed, as displayed in Fig. 43 (always in the case of a logic inverter). Aside from the resistive pull-up load, these three main NMOS circuit topologies are common, based on: a) two n-type TFTs, one of which acting as a diode load (Fig. 43a), b) a pseudo-CMOS circuit with two different supplies ($V_{DD}$ and $V_B$) and three additional TFTs (Fig. 43b), and c) a more complicated architecture with DG TFTs (Fig. 43c) gated at different $V_{GS}$. Even if shown only in the case of a logic inverter, all the above mentioned configurations (Fig. 42a and Fig. 43a-c) apply for digital, as well as analog circuits. Among the three possibilities with an active pull-up, the diode load configuration (Fig. 43a) presents the lowest complexity and area occupation, at a cost of a lower performance if compared to the pseudo-CMOS and DG configurations (Fig. 43b-c). In contrast, the pseudo-CMOS and DG configurations yield better performance (especially gain) at the cost of larger area occupation and more complicated fabrication processes. Despite the improved gain of both pseudo-CMOS and DG configurations, the (DC) power consumption is not reduced with respect to the diode load. The high power budget necessary for unipolar circuits is further increased in the case of flexible unipolar metal oxide semiconductor-based circuits by the use of typical $V_{DD}$ in the range of 5 V to 20 V, with some circuits operated at up to 50 V.

Circuit operation: In IV B and IV C, flexible digital and analog metal oxide semiconductor-based circuits employing unipolar or complementary configurations will be reviewed. To simplify the understanding of these subsections, we provide first an overview of the main performance parameters of digital and analog circuits.

Digital circuits: Fig. 44 displays the simplest and most straightforward example of a digital circuit, a voltage inverter (also known as NOT gate). The NOT gate is given in its complementary configuration, with both n- and p-type TFTs, but it can be realized in all the other unipolar circuit configurations shown in Fig. 42a and Fig. 43. The inverter function consists in taking the voltage signal applied at its input, inverting its voltage
levels, and providing the inverted signal at its output (OUT), as illustrated by its IN-OUT curve (see Fig. 44 b), also known as DC voltage transfer characteristics (VTC). From the VTC of a NOT gate, several specific DC parameters can be defined (see Fig. 44b):

- voltage input low (\(V_{IL}\)), which is the lowest input voltage where the slope of the VTC equals -1,
- voltage input high (\(V_{IH}\)), which is the highest input voltage where the slope of the VTC equals -1,
- voltage output high (\(V_{OH}\)), which corresponds to the output voltage at \(V_{IL}\),
- voltage output low (\(V_{OL}\)), which corresponds to the output voltage at \(V_{IH}\),
- maximum output swing (\(V_{L}\)), which is given by \(V_{OH} - V_{OL}\),
- midpoint voltage (\(V_{M}\)), which is the input voltage at which the NOT gate yields the same input and output level. Ideally \(V_{M}\) should be equal to \(V_{DD}/2\).

Additionally, from the VTC also the maximum and the minimum output voltages, \(V_{MAX}\) and \(V_{MIN}\) respectively, can be extracted. Other important parameters are the DC noise margins (NMs): the high (\(NM_H\)) and the low (\(NM_L\)) noise margin, which are the voltage ranges ensuring that a logic '0' or '1' is interpreted correctly also by a second inverter connected in cascade to the first one. They are defined as follows:

\[
NM_L = (V_{IL} - V_{OL}), \tag{IV.1}
\]

\[
NM_H = (V_{OH} - V_{IH}). \tag{IV.2}
\]

Another important DC parameter is the DC gain (\(G\)), which is the slope of the VTC when \(V_{IN} = V_M\). High noise margins and gain, together with a nearly "rail-to-rail" output (\(V_L \approx V_{DD}\)) are desirable. Together with the DC VTC, also the transient characteristics is important to determine various time constants, such as the rise and fall times (\(t_r\) and \(t_f\), respectively), as well as the propagation delay \(t_p\) (Fig. 45). As visible in Fig. 45, in a NOT gate (and in any other digital circuit), there is always a delay between the switching of the input and the output signal. For instance, \(t_r\) (\(t_f\)) are defined as the time needed for the output signal to switch from a logic '0' ('1') to a logic '1' ('0') (usually measured between the 10% and 90% of the output levels). The \(t_p\) is the time required for an output signal to change given a specific input transition (usually measured at the 50% levels of input and output voltage). Together with the NOT gate, also ring oscillators are important for determining the maximum switching speed of a digital gate given one output load. Ring oscillators comprise an odd number of NOT gates (the so-called delay stages) connected in a closed loop chain, resulting in an output signal oscillating between two limits (HIGH and LOW). The frequency of oscillation (\(f_o\)) of a ring oscillator depends on the number of delay stages (\(m\)) and the \(t_p\) of each stage:

\[
f_o = \frac{1}{2 \cdot m \cdot t_p}. \tag{IV.3}
\]

Another important parameter directly linked to the \(f_o\) is the ring oscillator stage delay, which is simply the double of the \(t_p\). The stage delay and the frequency of oscillation are typically used to estimate the (digital) switching characteristics of TFTs, especially in view of larger digital circuits. Finally, another key performance parameter for ring oscillators (and in general for digital circuits) is the power consumption \(P\), which is strictly linked to the \(f_o\):

\[
P = f_o \cdot C \cdot V_{DD}^2 \tag{IV.4}
\]
where C is the sum of the capacitances at the output node.

Analog circuits: The simplest flexible metal oxide semiconductor-based analog circuit is a single-stage common-source (CS) amplifier (see Fig. 46c), which acts as a voltage or transconductance amplifier. Flexible metal oxide semiconductor-based common-source amplifiers (as well as all other amplifier types) are usually designed in an unipolar configuration with an active n-type TFT (mainly IGZO) and different pull-up loads (see Fig. 42a and Fig. 43). The dynamic performance of a common-source amplifier (and of any other type of amplifier) is evaluated using the so-called Bode plot (amplitude and phase) shown in Fig. 46a-b, which is a standard format for plotting the circuit frequency response. On the horizontal axis, the frequency of the input voltage is in logarithmic scale, whereas on the vertical axis the amplitude and phase of the output voltage are respectively in decibel (dB) and degrees (deg). The amplitude of the amplifier in dB ($A_{dB}$) is given by following formula:

$$A_{dB} = 20 \cdot \log_{10} \left( \frac{V_{out}}{V_{in}} \right), \quad (IV.5)$$

where $V_{in}$ and $V_{out}$ are the amplifier input and output voltage, respectively. The Bode plot allows extracting several key circuit parameters:

- the DC gain (G), which is given by the amplifier amplitude at low frequencies,
- the cutoff frequency ($f_c$), which is the frequency at which $A_{dB}$ drops by 3 dB (-30%),
- the gain bandwidth product (GBWP), which is also called unity gain bandwidth as it is the frequency at which the amplification falls to unity.

For feedback configurations (e.g. operational amplifiers), instead of G, the open-loop gain ($G_{OL}$) is defined as the gain obtained in absence of feedback.

B. Flexible unipolar circuits

In this subsection, state-of-the-art flexible unipolar metal oxide semiconductor-based circuits (digital and analog) will be revised. First of all, the materials and the fabrication techniques employed will be reported, followed by the presentation of the electrical and mechanical properties of both digital and analog metal oxide semiconductor-based circuits.

Materials and fabrication techniques: Flexible metal oxide semiconductor-based circuits are typically unipolar, mainly based on n-type vacuum-deposited IGZO or ZnO active layers. Solution-processed metal oxide semiconducting materials are only rarely used for circuits, and in any case only for unipolar inverters or ring oscillators. As gate dielectrics Al$_2$O$_3$ or SiO$_2$ are mostly utilized, whereas source and drain electrodes are typically made of different metals like Au, Ti, Cr, and Cu, which can even be treated with special techniques (e.g. hydrogen plasma treatments) to reduce the contact resistance. Most common substrates are PI, PET, PEN and parylene.

Electrical properties: In the following, we will revise the electrical properties of flexible unipolar metal oxide semiconductor-based circuits. In particular, the circuit simulation and modeling will be first presented, followed by the experimental results obtained for both digital and analog circuits.

Simulation and modeling: The development of complete flexible TFT-based circuits requires a complete simulation of the AC and DC electrical performance, together with a precise modeling of the device mechanical properties. To this aim, the device DC characteristics needs to be extracted from the transfer and output curves measured for the fabricated TFTs. Additionally, it is also important to obtain the AC characteristics of the TFTs by measuring the device S-parameters and subsequently extracting the $f_T$, as explained in the previous sections. In this way, by fitting the coefficients of a TFT simulation model to the measured DC and AC characteristics, the performance of the circuits can be simulated before they are fabricated. Typical models used for such simulations are HSpice templates which can then be used in commercial circuit design tools for circuit analysis. One example of such a HSpice model is shown by Perumal et al., who fitted the model coefficients to the input, output and frequency measurements of a fabricated IGZO TFT.
[see II.B) and Fig. 21].

Nevertheless, the model by Perumal et al. is only valid for channel lengths down to 3.6\textmu m, with smaller channels needing an adaptation of the coefficients. To prove the validity of this model, Perumal et al. also demonstrated that a simulated 2-stage cascode amplifier behaves like the measured one. Similarly, Zysset et al. used a HSpice model to predict the performance of an IGZO-based operational amplifier prior to circuit fabrication. In particular, Zysset et al. also noticed the importance of modeling the parasitic capacitances caused by the pads and trace crossings at different layers of the circuit. In contrast to the electrical modeling of the circuits (which has been extensively investigated), the influence of mechanical bending has rarely been taken into consideration in the circuit design. Nevertheless, strain-induced effects should definitively be included in the TFT modeling, especially considering that the carrier mobility changes by \( \approx 2.5\% \), and \( V_{TH} \) by around 20 mV to 200 mV for \( \epsilon = 0.5\% \). Such changes can impact especially the performance of analog circuits and should be taken into consideration during the design process. To date, only Ma et al. has shown a HSpice-based simulator, which is able to include the threshold voltage variations induced by mechanical strain, as well as process modifications and aging.

**Digital circuits**: The majority of flexible metal oxide semiconductor-based circuits is constituted by NOT gates, and test structures like ring oscillators. Flexible unipolar vacuum-processed ZnO NOT gates on PI employing a diode load can typically achieve gains up to 2.5 V/V at 20 V supply (voltage output swing \( V_L \approx 17.5 \text{V} \)). Similarly, a vacuum-processed ZnO NOT gate on PI foil with a gain of 1.5 V/V at a supply voltage of only 9 V was also demonstrated. Additionally, also NOT gates with resistive pull-up loads employing solution-processed metal oxide semiconductors have been reported, like ion-gel gated ZnO NR NOT gates on paper yielding a gain of 2 V/V at a supply voltage of 1.3 V, and aerosol-jet printed ZnO NOT gate on PI with gain up to 8 V/V (\( V_{DD} = 2 \text{V} \)).

Interestingly, Karnaušienko et al. demonstrated IGZO-based NOT (and NAND) gates that were able to roll up to a radius of 25\textmu m after fabrication and release. Recently, also 2 TFT/1 Capacitor (2T1C) display drivers based on IGZO TFTs on PEN or PI foil and capable of driving OLED pixels at a frame rate >60 Hz were shown. A larger number of TFTs is employed for ring oscillators, whose stage delay is typically used to determine the maximum switching speed that can be achieved in larger digital gates. Fig. 47 displays the stage delay (with respect to the supply voltage) obtained for a number of published flexible ring oscillators based on vacuum-deposited metal oxide semiconductors. The lowest stage delay was achieved with ZnO ring oscillators, which yielded a 16 ns delay at 18 V supply voltage. Already at 2 V supply voltage, the delay of the same ring oscillators increased to \( \approx 300 \text{ns} \). The smallest RO is composed by 3 stages of IGZO TFTs on a metal foil and oscillates at \( f_o = 360 \text{kHz} \) (stage delay of 926 ns) with a supply voltage of 15 V. Increasing the supply voltage to 50 V raises the oscillation frequency to 1.14 MHz and results in a stage delay of 291 ns. A larger IGZO RO (5 stages) oscillating at 182 kHz at 20 V (stage delay of 550 ns) and \( f_o = 572 \text{kHz} \) at 30 V (stage delay of 350 ns) was reported by Hsieh and Wu on PI foil. Such a low stage delay is partially a result of the use of a substrate with a high \( T_C \approx 350 \text{°C} \), allowing a high temperature annealing of the IGZO film (and therefore an improved TFT performance). For display applications, flexible metal oxide semiconductor-based shift registers are also commonly utilized. Mativenga et al. reported a 5 IGZO TFT shift register (operated at 19.7 V) yielding a rise time \( t_r \) of 0.9\textmu s and a fall time \( t_f \) of 0.8\textmu s based on 15\textmu m colorless PI. Interestingly, Nelson and Tutt presented 7-stage ring oscillators based on flexible ZnO TFTs with 400 ns stage delay at 5.5 V supply voltage (and 6\textmu s at 1.5 V). Flexible 7-stage ring oscillators based on solution-processed metal oxide semiconductors have also been reported recently. The smallest delay of \( \approx 100 \text{ns} \) (at 15 V \( V_{DD} \)) obtained for sol-gel \( \text{In}_2\text{O}_3 \) ring oscillators on PI. Even more stages (11) have been shown by Mativenga et al., who demonstrated an IGZO RO working at 94.8 kHz at 20 V, resulting in a stage delay of 480 ns on PI or PET substrates. The same publication also presented a two clock shift register with 10 TFTs and 1 Capacitor per stage, which is suitable for display applications. Further increasing the number of stages, Zhao, Mourey, and Jackson showed a ZnO 15-stage RO with 16 ns delay at 18 V and 300 ns delay at 2 V. The realization of a flexible 19-stage IGZO RO with a stage delay of 19 ns at 20 V was only
possible due to the low TFT contact resistance that was achieved between source/drain and IGZO.\textsuperscript{315} Even more TFTs were utilized for an AMOLED line driver based on IGZO capable of 45 frames/s at 11 V on PEN foil, which has also been integrated with an optical display (64 × 160 pixels) and a 2T1C pixel driver circuit.\textsuperscript{308,309} At a supply voltage of 15 V, the flexible line driver consumed a power of ≈97 µW.\textsuperscript{308,309} Similarly, Zhang et al. reported a 48 stage scan driver based on IGZO with an output swing of 16 V at 100 kHz.\textsuperscript{186} Even larger TFT count have been reported in combination with RFID or near field communication (NFC) applications. For example, Myny et al. demonstrated an IGZO based NFC tag consisting of an high frequency (HF) capacitor, a 19-stage ring oscillators acting as a clock source, a 4-bit modulo-12 counter, a 12-bit decoder and several out registers and buffers all integrated on the same foil and laminated on top of an antenna coil.\textsuperscript{314} The flexible NFC code generator was capable of transmitting data at 71 kB s\textsuperscript{−1}, given enough supply voltage.\textsuperscript{314} Based on this design, three different pull-up load configurations (diode load, pseudo-CMOS, DG) were compared, as shown in Fig.48.\textsuperscript{314} The TFT count ranges between 218 and 436 TFTs.\textsuperscript{314} Similarly, Tripathi et al. demonstrated an IGZO-based RFID code generator (8-bit) operating at 6.4 kB s\textsuperscript{−1} (2 V supply voltage) fabricated on PEN foil. The RFID code generator by Tripathi et al. was constituted by 300 flexible IGZO TFTs, resulting in an occupied area of 51.7 mm\textsuperscript{2}.\textsuperscript{324} The most recent work on RFID circuits was done by Myny and Steudel with an near field communication (NFC) transponder with 438 IGZO TFTs on 10.884 mm\textsuperscript{2} on a polyimide foil substrate. With a datarate larger than 14.3 kB s\textsuperscript{−1} and at most 396.5 kB s\textsuperscript{−1} this circuit complies with the ISO 14443 NFC standard\textsuperscript{317}.

**Figure 49.** DC gain versus gain bandwidth product (GBWP) of recently reported flexible metal oxide semiconductor-based analog amplifiers.
(with a single active IGZO TFT) yield a DC gain of 86.5 dB at a cut-off frequency of 8.38 kHz (when supplied at 5 V). Tai et al. utilized 2 flexible IGZO DG TFTs to realize a flexible differential amplifier with 20 dB DC gain at a cut-off frequency of ≈300 Hz ($V_{DD} = 10.5$ V). A similar IGZO amplifier with lower DC gain of 2 dB and higher cutoff frequency of ≈1 MHz was also fabricated on a 1 µm parylene foil. Similarly, Shabanpour et al. presented a flexible IGZO-based cascode amplifier with a DC gain of 10.5 dB and a cutoff frequency of 2.62 MHz (GBWP ≈ 8.8 MHz) at 6 V supply. The cascode amplifier by Shabanpour et al. consumes 762 µW power during standard operation. A second version of this cascode amplifier showed a higher DC gain (25 dB) at the cost of a lower cut-off frequency of 220 kHz, consuming 2.32 mW power at 6 V. Even more TFTs (13 IGZO devices) were needed to realize an operational amplifier with a GBWP of 31 kHz and an open-loop gain $G_{OL}$ of 22.5 dB, resulting in a $f_c = 5.6$ kHz. Furthermore, this operational amplifier consumed 160 µW power during standard operation. Similarly, Shabanpour et al. showed a 2-stage Cherry-Hooper amplifier yielding a DC gain of 33 dB at a cutoff frequency of 400 kHz, resulting in a GBWP of 18.5 MHz based on IGZO TFTs. During the circuit measurements, the Cherry-Hooper amplifier was supplied with 6 V, consuming 4.96 mW power. Chung et al. realized an alpha particle detecting circuit by AC coupling 4 different stages of amplification employing 14 active IGZO TFTs. The circuit by Chung et al. yields a linear DC gain of 14.9-20 V/V and a band-pass characteristic. In a similar fashion, simulations of different band-pass topologies were shown by Bahubalindrumi et al. with simulated DC gains of up to 75 dB and cut-off frequencies in the order of 25 MHz. The flexible metal oxide semiconductor-based analog circuit with the largest TFT count is an operational amplifier with 16 IGZO TFTs. This amplifier is supplied at 5 V and presents a DC gain of 18.2 dB at a cut-off frequency of 108 kHz (the circuit layout and Bode plot is shown in Fig. 50).

Mechanical properties: The realization of reliable flexible (and bendable) metal oxide semiconductor-based circuits is challenged by the dimensional instability of the flexible substrates (e.g. expansion/shrinking occurring during the fabrication process). Due to the substrate deformation, large tolerances are necessary while aligning the different device layers (especially gate with respect to source/drain electrodes). Therefore, the maximum operating frequency of the circuit, as well as the total circuit area are limited. Another key challenge in the realization of flexible circuits is constituted by the mechanical strain that is induced in the flexible TFT channels when the substrate is bent. As already explained, the goal is the fabrication of flexible metal oxide semiconductor-based circuits as strain resistant as possible, and at the same time also with the smallest strain-induced performance parameter variations. Regarding strain resistance, as shown in equation II.1, the minimum bending radii depend directly on the thickness of the substrate and of the other device layers (materials and thicknesses). Depending on the device layer stack and thicknesses, the typical bending radii range from 30 mm down to 50 µm (demonstrated for a differential amplifier on 1 µm parylene substrate). While strain resistance limits the application range of the circuits, strain-induced TFT performance parameters can severely compromise the circuit functionality, especially when the occupied area is large (as for digital circuits). Prior to the circuit fabrication, it is indeed important to account for the bending-induced variations each single TFT is subjected to by simulating the mechanical TFT behaviour and by modeling/designing the circuit topologies. In particular, there are several approaches that allow mitigating strain-induced performance variations. Firstly, all the TFTs can be aligned parallel to each other in order to present the same strain-induced variations, as well as resistance to bending all over the circuit structure. This approach has been first proposed by Münzenrieder et al., who demonstrated that 5-stage ring oscillators constituted by IGZO devices all aligned parallel to each other show only small performance decrease when mechanically bent to $\epsilon = 0.72 \%$. By aligning parallel to each other all the 40 TFTs of a 8-stage 5 TFT shift register, Mativenga et al. demonstrated an almost negligible parameter shift of the circuit down to radii of 4 mm. Moreover, by employing a 25 µm-thick PEN foil and an encapsulation layer shifting the neutral strain axis close to the TFT stack, Tripathi et al. realized an 8 bit code generator yielding negligible parameter shift for tensile bending at a radius of 2 mm. Additionally, also the circuit design can be selected in a way to achieve a performance based on the ratio of the same TFT performance parameters. Such approach applies especially for analog circuits...
circuits, which can be designed to yield a gain depending only on the ratio of the transconductance of the different TFTs, and not on a single transconductance. Using this technique for an operational amplifier based on 16 IGZO all aligned parallel to each other, Zysset et al. realized a flexible circuit yielding a strain-independent DC gain and bandwidth (at a radius $R = 5 \text{ mm}$).\textsuperscript{211}

### C. Flexible complementary circuits

All the results presented in IV B have been obtained with unipolar circuits, employing mainly flexible n-type vacuum-processed metal oxide semiconductor TFTs. Even if excellent performance can be achieved with unipolar circuitry, key issues such as low-power consumption, as well as easy and compact circuit design can be only accomplished by complementing n- with p-type TFTs. Nevertheless, to realize flexible metal oxide semiconductor-based complementary circuits, flexible n- and p-type devices with similar performance (especially mobility) are required. This is especially challenging in the case of metal oxide semiconductors, due to the typically low carrier mobility values that can be obtained for flexible p-type devices (see section III).

For this reason, only few groups have reported flexible complementary circuits (mainly digital circuits) based on both n- and p-type metal oxide semiconductor-based TFTs.\textsuperscript{79,176,271,284} To overcome this bottleneck, other technologies have been considered to realize the p-type channel. For instance, organic semiconductors have well-known hole transporting properties, with sufficient carrier mobility. Thus, different combinations of p-type organic TFTs with n-type metal oxide semiconductor TFTs have so far been demonstrated on flexible substrates.\textsuperscript{103,171,329–331,339–341} In the following, the materials and fabrication techniques, as well as the electrical and mechanical properties of flexible complementary circuits based on both fully metal oxide semiconducting materials, as well as hybrid organic-metal oxide semiconductors are reviewed.

#### Materials and fabrication techniques

The materials and fabrication processes employed for flexible complementary metal oxide semiconductor-based circuits are similar to the materials and techniques mentioned previously, except that the channel is made by two different semiconducting materials. Common substrates used for flexible complementary circuits include: paper,\textsuperscript{79,271} PES,\textsuperscript{284,329,330,339} PI,\textsuperscript{103,171,176,331,342,343} PET,\textsuperscript{340,341} and PDMS.\textsuperscript{331} In addition to the substrate, sometimes a barrier, buffer or encapsulation layer is deposited in order to improve electrical isolation, decrease surface roughness and increase stability, like inorganic Si$_n$N$_x$ adhesion layers,\textsuperscript{103} and organic Cytop\textsuperscript{103} or AZ1518\textsuperscript{103} encapsulation films. Most widely used gate dielectrics for flexible complementary circuits are AlO$_x$,\textsuperscript{329} Al$_2$O$_3$,\textsuperscript{103,284,331,339,342,343} SiO$_2$,\textsuperscript{331,342,343} PVP,\textsuperscript{171} Si$_3$N$_4$,\textsuperscript{330} and HfO$_2$.\textsuperscript{176} As metal oxide semiconductors provide good n-type transport, the n-channel is always made of a metal oxide semiconductor deposited via RF-magnetron sputtering.\textsuperscript{79,103,171,176,271,284,329–331,339–343} or SP\textsuperscript{103,144} on flexible substrates at compatibly low temperatures. Best performing n-type metal oxide semiconductors include IGZO,\textsuperscript{79,103,171,284,330,331,339–343} ZnO,\textsuperscript{176,329} and In$_x$O$_y$.\textsuperscript{103,144} On the other hand, the p-channel is either formed by a metal oxide\textsuperscript{271,284} or an organic semiconducting material.\textsuperscript{103,171,329–331,339–343} As p-channel metal oxide semiconductor materials, till now only SnO$_2$,\textsuperscript{79,176,271} and Cu$_2$O\textsuperscript{284} deposited by RF-magnetron sputtering have been employed. In the case of organic p-type semiconductors, several materials have been used, employing solution-processable, low temperature, scalable and cost-effective techniques such as ink-jet printing,\textsuperscript{340,341} spin-coating,\textsuperscript{103} and dip-coating,\textsuperscript{331,342,343} in addition to the widely used thermal evaporation with shadow masking.\textsuperscript{171,329,330,339}

Different groups have so far demonstrated the potential of integrating p-type pentacene,\textsuperscript{171,329,330,339} poly-(9,9-dioctylfluorene-co-bithiophene) (F8T2),\textsuperscript{340,341} and semiconducting single walled carbon nanotubes (SWCNTs)\textsuperscript{103,331,342–344} with n-type ZnO,\textsuperscript{329} In$_x$O$_y$,\textsuperscript{144} and IGZO.\textsuperscript{103,171,330,331,339–343}

#### Electrical properties

Compared to unipolar circuits, the range of reported flexible complementary metal oxide semiconductor-based circuits is smaller. The majority of the published complementary circuits are digital, especially NOT, NAND and NOR gates, and ring oscillators based both on p- and n-type metal oxide semiconductors and on hybrid p-type organic and n-type metal oxide semiconducting materials. Additionally, also two common-source amplifiers and one differential amplifier have been reported.\textsuperscript{271,342}

#### Digital circuits

The first example of flexible complementary metal oxide semiconductor-based circuit is dated 2008, when Oh et al. demonstrated the integration of pentacene and ZnO TFTs to realize a mechanically flexible complementary NOT gate on PES with a gain of 100 V/V and a low voltage operation.\textsuperscript{329} The dynamic behavior of the hybrid pentacene/ZnO complementary NOT gate showed an $f_n$ of 5 Hz.\textsuperscript{329} In 2010, Kim et al. demonstrated a pentacene/IGZO complementary NOT gate on PES with a gain up to 165 V/V centered at $V_M = 14$ V ($V_{DD} = 30$ V).\textsuperscript{330} In 2011, Kim et al. reported vertically stacked pentacene/IGZO NOT gates.\textsuperscript{339} Furthermore, they also showed also mechanically bendable pentacene/IGZO NOT gates.\textsuperscript{171} Alternatively to pentacene devices, Nomura et al. exploited p-type F8T2 TFTs in a vertically stacked geometry on top of ZnO devices, employing a common gate electrode on PET.\textsuperscript{341} The F8T2/IGZO NOT gate showed a gain $G = 100$ V/V at a maximum
supply of 30 V. The same group realized also vertically stacked FST2/IGZO NAND gates on PET. In 2011, the first fully metal oxide semiconductor-based NOT gates were presented, employing n-type IGZO and either p-type CuO$_x$ or SnO$_x$. In particular, Dindar et al. presented vertically stacked CuO$_x$/IGZO NOT gates on PES, yielding a high gain of 120 V/V with a nearly “rail-to-rail” output swing. Employing n-type IGZO and p-type SnO$_x$ TFTs on a flexible paper substrate (acting also as gate dielectric), Martins et al. showed NOT gates with a maximum G = 4.5 V/V at VM of 3.6 V (V$_{DD}$ = 17 V). This structure was later improved with an optimized geometric aspect ratio (W/L)$_p/(W/L)_n$, which enabled also the realization of NAND and NOR logic gates. Recently, solution-processed semiconducting SWCNTs have also been exploited as p-type TFTs and integrated into flexible complementary circuits with n-type sputtered IGZO or spray coated In$_2$O$_3$ TFTs. Mechanically bendable hybrid SWCNT/IGZO NOT gates on PI showed a maximum gain of 87 V/V, a nearly perfectly centered VM and a “rail-to-rail” VL (Fig. 51). In addition, Petti et al. exploited also the use of spray-coated In$_2$O$_3$ as n-type semiconductor and presented SWCNT/In$_2$O$_3$ NOT gates with a lower gain of SWCNT/In$_2$O$_3$ NOT gates with a lower gain of 22 V/V. The reduced performance of the SWCNT/In$_2$O$_3$ NOT gates was mainly attributed to the poorer performance of the solution-deposited In$_2$O$_3$. Using SWCNT and IGZO TFTs, Chen et al. successfully realized large-scale complementary circuits (NOT, NAND and NOR gates, as well as ROs) on PDMS comprising a large TFT count. Fig. 52 a-b) show the optical micrograph and output characteristic of the 501-stage hybrid SWCNT/IGZO complementary RO with up to 1004 TFTs, yielding an f$_o$ of 294 Hz. Finally, Honda et al. presented mechanically bendable NOT, NAND and NOR gates based on SWCTN and IGZO TFTs on PI. The SWCNT/IGZO NOT gate showed a gain of 45 V/V and a low t$_r$ = 0.75 ms. The same group, also realized 3D vertically-integrated SWCNT/IGZO NOT gates with similar performance. Very recently, Li et al. demonstrated a flexible CMOS 5-stage ring oscillator based on n-type ZnO TFT and p-type SnO$_x$ TFT, with a maximum oscillation frequency of 18.4 kHz.

Analog circuits: As regards flexible metal oxide semiconductor-based analog circuits, Martins et al. reported common-source and differential amplifiers (see Fig. 53) with a gain of 16.3 V/V and 4.1 V/V respectively, based on the same optimized device structure employed to realize the SnO$_x$/IGZO NOT, NAND and NOR gates on (and with) paper. Based on the previously mentioned 3D vertically-integrated SWCNT/IGZO TFT structure shown by Honda et al., common-source amplifiers with a gain G > 5 dB have also been fabricated.
Mechanical properties: In addition to the electrical DC and AC characterization, also bendability influences the device performance. Several groups\textsuperscript{103,171,176,329,342,343} have characterized hybrid complementary NOT gates under tensile bending, down to radii of 2.6 mm ($\epsilon = 1.25 \%$),\textsuperscript{342} showing only minor variations. Oh et al. reported mechanical bending tests of pentacene/ZnO NOT gates at bending radii of 56 mm with high gain of 100 V/V.\textsuperscript{329} The hybrid pentacene/IGZO complementary NOT gate demonstrated by Kim et al. yielded a maximum gain of 60 V/V at a bending radius of 6 mm.\textsuperscript{171} Furthermore, hybrid SWCNT/IGZO complementary NOT gates have proven to be functional, with a maximum gain of 87 V/V even when bent to a tensile radius of 10 mm ($\epsilon = 0.29 \%$), as shown in Fig. 51.\textsuperscript{103} Additionally, Honda et al. proved also the functionality of both the planar and the 3D vertically-integrated SWCNT/IGZO NOT gates down to tensile bending radii of 2.6 mm, with a maximum gain of 50 V/V and a low voltage operation.\textsuperscript{342,343} Finally, Li et al. successfully characterized ZnO/SnO$_2$ CMOS inverters under tensile and compressive strain.\textsuperscript{176} In particular, a small gain reduction was observed under tensile strain, while the influence of compressive strain was demonstrated to be negligible.\textsuperscript{176}

V. METAL OXIDE SEMICONDUCTOR-BASED SYSTEMS

The improvements recently achieved in the electrical (DC and AC) and mechanical performance of flexible metal oxide semiconductor TFTs, combined with special features like transparency, stretchability, conformability, dissolubility, and mechanical activity envision a wide range of possible applications that go beyond optical displays. Even if the research in this area has only shown significant advances in the last years, already quite a few systems have been developed and brought at least to a prototype stage. This section will exemplary list the progresses achieved in the field of flexible metal oxide semiconductor-based electronics, covering systems for optical displays, sensors, power transmission, as well as data storage and transmission.

Optical display systems: Optical displays are still the main driving application for metal oxide semiconductor TFTs. Recently many prototypes of flexible optical displays, especially AMOLED, based on metal oxide semiconductor TFT-based backplanes, have been published. The majority of the reported display systems employ vacuum-processed IGZO TFTs\textsuperscript{39,40,126,157,174,175,202,309,315,345–351} on PEN,\textsuperscript{40,126,157,309,347–351} PI,\textsuperscript{315,345–347} or PEEK foils.\textsuperscript{202,347} Besides IGZO, also other multicomponent vacuum-processed metal oxide semiconductors like ITZO have been utilized to realize flexible displays.\textsuperscript{126} Among the various demonstrated systems, in 2013 Chida et al. reported a mechanically flexible 3.4-inch top-emitting AMOLED display yielding 326 pixels per inch (ppi) resolution and consuming 570 mW power.\textsuperscript{39} Additionally, the display by Chida et al. was operational after 1000 bending cycles at 5 mm bending radius. One year later, Genoe et al. proposed the use of a digital pulse width modulation (PWM) to drive a flexible top-emitting AMOLED display (0.54-inch, 320 ppi).\textsuperscript{309} The PWM concept presented by Genoe et al. allowed reducing the DC power consumption down to 102.4 mW.\textsuperscript{309} Recently, Motomura, Nakajima, and Takei proposed the use of air-reactive electrode-free inverted OLEDs (iOLEDs) in flexible IGZO TFT-driven AMOLEDs (8-inch, 100 ppi) to suppress typical undesired effects like dark spot growth and achieve longer lifetimes.\textsuperscript{126} Although the iOLED characteristics were inferior to those of conventional OLEDs, the flexible display by Motomura, Nakajima, and Takei yielded stable and clear moving images even while bent.\textsuperscript{126} Recently, Nag et al. successfully demonstrated the integration of a flexible quarter-quarter-video-graphics-array (QQVGA) AMOLED display (85 ppi) driven by self-aligned TG IGZO TFTs.\textsuperscript{315} The resulting flexible display required only five lithographic mask steps and resulted in a total thickness of $\approx 150 \mu$m.\textsuperscript{315} Fig. 54a displays a photograph of the entire system on PI, whereas Fig. 54b shows the display with an image applied.\textsuperscript{315} Komatsu et al. demonstrated a flexible AMOLED displays (3.4-inch, 249 ppi) with a CAAC IGZO TFT backplane. The flexible display by Komatsu et al. was functional after $\leq 70,000$ folding cycles at 1 mm radii.\textsuperscript{175} Employing this structure, Komatsu et al. fabricated a 5.9-inch foldable book-type AMOLED display, as well as a 5.9-inch tri-foldable AMOLED display for smartphone applications.\textsuperscript{175} Beyond AMOLED displays, also a (smaller) woven textile display employing LEDs (3x3-matrix) actuated by flexible IGZO TFTs have been realized, showing the feasibility of this technology also for smart textile applications.\textsuperscript{213}
Sensoric systems: Several sensoric systems, based on metal oxide semiconductor TFTs, have been demonstrated, e.g. for biochemical, temperature, and image sensing.

Biochemical sensors: Flexible and stretchable metal oxide semiconductor devices are attracting an increasing interest especially in the field of epidermal electronics,13,15 smart implants,352 artificial electronic skins for robots,19 as well as food safety and water monitoring.165 In order to enable these applications, biochemical sensors are necessary. Recently, Liu et al. reported a metal oxide semiconductor TFT-based pH sensor on PET (Fig.55).184 The pH sensor is based on an electrolyte gated IZO neuron device, i.e. a TFT with multiple input gates that are capacitively coupled to a floating gate, as proposed by Shibata and Ohmi.353 In the work by Liu et al., the $V_{TH}$ shift of the flexible IZO neuron TFT was employed to detect pH changes with a sensitivity of around 105 mV/pH.184 Fig.55 shows the sensor structure, together with a micrograph and a photograph of the entire system (reproduced from Liu et al. with the permissions from Nature Publishing Group).184

Temperature sensors: To continuously monitor the temperature of temperature-sensitive AMOLEDs or AMFPDs, flexible metal oxide semiconductor TFT-based temperature sensors are required. To this regard, an interesting approach has been proposed by Honda et al. who vertically integrated a printed temperature sensor constituted by a SWCNT and poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) conductive sensor ink on top of a SWCNT/IGZO CMOS NOT gate, as shown in Fig.56.342 The flexible temperature sensing system yields a sensitivity of 0.68 %°C$^{-1}$ and a resolution $\leq$ 0.3 °C, and is functional while bent to 2.6 mm tensile radius.342 The high density integration (only 4µm passivation layer) paves the way to highly integrated and high-performance flexible devices for practical applications, e.g. wearable health monitoring.

X-ray detectors: Another interesting and novel field of application for metal oxide semiconductor TFTs is represented by flexible x-ray detectors.354 In 2012, Lujan and Street reported a flexible flat panel (FP) x-ray detector array based on flexible IGZO TFTs on PET.354 The device operated in indirect detection mode, and was based on the integration of a phosphor layer, an a-Si continuous photodiode and an IGZO TFT backplane. In the device, the x-rays incident on the phosphor layer excited fluorescence, which was subsequently detected and imaged by the a-Si photodiode and TFT backplane. In this way, images with a resolution of 160 x 180 pixel and pixel size of 200µm could be recorded. Fig.57 shows an image recorded with the flexible FP x-ray detector array. Few years later, also Smith et al. reported large-area flexible x-ray detectors based on a-Si continuous photodiodes and IGZO TFT backplanes on 125µm PEN foils. In this work, Smith et al. proposed a novel assembly technique that allowed connecting single flexible x-ray detectors to create a larger composite x-ray detector (Fig.58).321 As visible from Fig.58, 9 x-ray detectors (each with 16 x 16 pixel resolution) were overlapped to create a larger detector array. The assembly technique can be scaled up to even larger x-ray imaging arrays enabling applications in the medical imaging, e.g., a single-exposure and low-dose digital radiography. In 2015, Gelinck et al. presented a flexible x-ray detector based on an organic photodetector (OPD) layer and an IGZO TFT backplane all integrated on...
will introduce two wireless power transmission systems diodes based on metal oxide semiconductors. Finally, we followed by an overview of state-of-the-art flexible p-n basic structure and operating principle of p-n diodes, nodes.

TFTs in diode load configuration (i.e. shorted gate-drain can be either implemented with p-n diodes, coils (source and receiver) and a rectifier circuit, which power transmission systems can be realized utilizing two

Figure 57. X-ray image obtained from an 80 kV exposure with a flexible flat panel x-ray detector array fabricated with an IGZO TFT backplane on PET. The black dots and lines are defects (reproduced from Lujan and Street with the permission from IEEE).

Figure 58. Large-area flexible composite x-ray detector constituted by a 3 x 3 active matrix array of 9 individual flexible x-ray detectors based on a continuous photodiodes and IGZO TFT backplanes (reproduced from Smith et al. with the permission from IEEE).

a 25 µm PEN foil. The use of a solution-processed OPD instead of an a-Si photodiode allowed reducing the number of photolithographic steps, opening the way to lower production costs. Using this flexible OPD/IGZO TFT x-ray detector, images with a resolution of 120 x 160 pixel and pixel size of 126 µm could be recorded at a high-resolution (10 frames/s). The flexibility of all these x-ray imaging systems allows realizing curved detectors for applications such as computed tomography, where a round detector is more beneficial.

Power transmission systems: Flexible wireless power transmission systems can be realized utilizing two coils (source and receiver) and a rectifier circuit, which can be either implemented with p-n diodes, or with TFTs in diode load configuration (i.e. shorted gate-drain nodes). In the following, we will first introduce the basic structure and operating principle of p-n diodes, followed by an overview of state-of-the-art flexible p-n diodes based on metal oxide semiconductors. Finally, we will introduce two wireless power transmission systems developed, based on elastic NiO/IGZO diodes, and flexible diode load IGZO TFTs.

Diodes: Diodes are electronic components with two terminals that conduct primarily in one direction. A p-n diode is realized by a p- and an n-type semiconductor brought in contact with each other to form a p-n junction. The p-n junction facilitates the current conduction exclusively in one direction, and suppresses the current flow in the other direction, acting thus as a rectifying element. Instead of a semiconductor-semiconductor junction, a Schottky diode possesses a metal-semiconductor junction. Here a Schottky barrier is formed, allowing the device to have a very high switching speed as well as a low forward voltage drop.

Metal oxide semiconductor diodes: Flexible metal oxide semiconductor-based p-n diodes have been realized employing n-type IGZ and either Cu$_2$O or NiO p-type semiconductors. In particular, Chen et al. reported a mechanically flexible Cu$_2$O/IGZO p-n diode on PEN. The authors demonstrated also the rectification characteristics of the Cu$_2$O/IGZO diode by converting an AC voltage of 4 V into a DC voltage of around 2.5 V. The -3 dB frequency of around 27 MHz (even while bent to R = 20 mm), allowed employing the rectifier even for HF applications. Utilizing IGZO and NiO semiconductors, Müenzenrieder et al. presented a mechanically bendable p-n diode fabricated at RT on PI. The rectification properties of the NiO/IGZO diode were shown even down to a R = 10 mm. The 4.7% increased rectified voltage for the bent NiO/IGZO diode as compared to the flat one. Flexible Schottky diodes which are based on metal oxide semiconductor have been demonstrated with different semiconductor materials, such as ZnO or a-IGZO. Specifically, Zhang et al. present a Ag/ZnO Schottky diode fabricated on ITO coated PET substrates. Even after bending down to a radius of 30 mm, the devices are still functional. Other work show IGZO-based Schottky diodes that convert 3 V AC voltage into a 1.7 V DC voltage with a cutoff frequency of 1.1 GHz. Zhang et al. even increase the cutoff frequency to 6.3 GHz which is well beyond the critical speed of 2.45 GHz for principal frequency bands for smartphones. Only recently, solution processed Schottky diodes based on ZnO have been shown by J. Semple, S. Rossbauer and K. Zhao, L. K. Jagadamma, A. Amassian, M. A. McLachlan, that have a cutoff frequency of well beyond 20 MHz. The solution processing will - in contrast to vacuum processing - allow the devices to become compatible with cost-effective large-volume production.

Diode-based power transmission systems: Utilizing a rectifier circuit constituted by 4 NiO/IGZO p-n diodes in a bridge configuration, Müenzenrieder et al. realized an elastic and conformable wireless power transmission
system (Fig.59a-b). In the system by Münzenrieder et al., an AC voltage is first transferred wirelessly via inductive coupling of two coils (source and receiver), and subsequently rectified by the diode bridge (Fig.59). The transmitted DC power of 450 µW while the receiver coil is lying within the source coil is sufficient to supply standard metal oxide semiconductor-based circuits. Furthermore, the wireless power transmission system is functional while conformably wrapped around an artificial hip joint (R = 14 mm), as shown in Fig.59c.

TFT-based power transmission systems: It is also possible to rectify a wireless transmitted AC voltage utilizing flexible IGZO TFTs in diode load configuration, as demonstrated by Myny et al. In this particular example, Myny et al. employed the rectified voltage to power an NFC tag on PET (typical transmitted power of ≈10 µW).

Data transmission systems: Aside optical display, one of the main application areas of flexible metal oxide semiconductor TFT is that of large-scale, cheap and disposable data transmission systems, such as RFID or NFC tags and smart labels. In this field, special features like transparency would even enable new application frontiers, such as flexible and transparent RFID/NFC tags seamlessly embedded in everyday objects like food and water packages, mirrors, windows, books.

NFC tags: Myny et al. demonstrated a flexible NFC tag based on at least 218 IGZO TFTs on PET. Details of the circuit block diagram can be found in IV-B. The flexible NFC tag was powered by inductively coupling it to a commercial USB-connected NFC reader (operating at 13.56 MHz and at a maximum distance of 5.2 cm). As a main result, Myny et al. demonstrated that the flexible IGZO-based NFC tag could meet the key requirements for RFID/NFC applications (e.g. power consumption, data rates, signal encoding).

Data storage systems: Storing data is also essential for flexible electronic systems. As already seen in the previous sections, ferroelectric P(VDF-TrFE) or chicken albumen gate dielectrics allow realizing non-volatile 1-bit memory elements. To this regard, Van Bremen et al. demonstrated a non-volatile memory array [16 x 16 IGZO TFTs with P(VDF-TrFE) gate dielectrics on PEN] with retention times of up to 12 days. The same group reported also the integration of a similar flexible non-volatile memory array (4 x 4) with a TFT addressing circuit (based on standard BG IGZO devices) that could read and write each single memory element of the array. The memory and logic TFTs share the Au S/D electrodes, as well as the IGZO semiconducting layer. It was shown that the IGZO TFT-based addressing circuit was able to successfully program/erase the 4 x 4 non-volatile memory array using 10 ns per memory element. Furthermore, a suitable voltage margin of 4 V between the ‘0’ and ‘1’ states allowed a fast and reliable read-out of the stored data.

VI. CONCLUSIONS

Flexible metal oxide semiconductor-based TFTs have not only made their entry in the market of optical displays, but they have also shown to be suitable for other novel electronic systems: e.g. for sensorics, power supplies, as well as data storage and transmission. This wide range of applicability of flexible metal oxide semiconductor technology is owed to its excellent electrical and mechanical properties, combined with unique features like transparency, light-weight, 3D conformability, stretchability, and/or solution-processability. In this paper, we reviewed the state-of-the-art of flexible TFTs, circuits and systems based on metal oxide semiconductors. Significant attention is devoted to aspects especially important for flexible devices: from the materials (i.e. substrates that are flexible, temperature- and chemical-resistant, etc.), the fabrication techniques (i.e. substrate preparation, low temperature deposition methods, layer structuring on dimensionally unstable substrate, etc.), the electrical performance, the mechanical properties (i.e. bendability, improvement of bendability) to special features (i.e. transparency, stretchability, dissolubility, etc.). The main part of the review described the currently available approaches to realize flexible TFTs based on vacuum-deposited n-type metal oxide semiconductors. However, also novel topics like solution-processing and hole conduction in flexible metal oxide semiconductor TFTs have been thoroughly reported. Given the recent progresses achieved in the large-area integration of flexible devices, a relevant part of the review deals with circuits, as well as systems.
based on metal oxide semiconductor TFTs. Examples of novel large-area flexible electronic systems include flexible, textile-integrated, rollable and/or foldable optical displays, \(^{39,40,126,157,174,175,202,213,209,315,345–351}\) flexible and/or stretchable systems for temperature, \(^{342}\) pH, \(^{165,184}\) and x-ray sensing, \(^{321,354,355}\) wireless power transmission, \(^{81,314}\) as well as non-volatile storage and NFC transmission of data. \(^{135,166,203,314}\) Despite the advances that flexible metal oxide semiconductor TFTs have witnessed in the last decade, there are still some bottlenecks that prevent the commercialization of this technology in new areas of application beyond optical displays. To broaden the field of application of flexible metal oxide semiconductor TFTs, future work should focus first of all on the optimization and establishment of the developed technology. In particular, specifically complete TFT models simulating both electrical and mechanical TFT properties are necessary to predict the performance under every circumstance, e.g. substrate fabrication, peeling and/or transferring, as well as bending and/or stretching. In addition to the development of suitable models, further advances in the material technology are also necessary. This means combining advanced flexible substrates (i.e. ultra-thin, light-weight, transparent, conformable, stretchable, biocompatible, biodegradable, and/or cheap) with suitable device layers (i.e. thin, ductile, transparent, biocompatible and/or biodegradable) to realize a broad range of flexible devices: from TFTs, circuits, sensors, display elements, actuators, to power supplies. Furthermore, with the help of suitable models, many efforts need to be devoted also in the heterogeneous integration of all these devices over large-area flexible substrates in order to achieve electrically and mechanically robust and reliable systems. Finally, future commercialization of flexible metal oxide semiconductor electronics calls for a reduction of the manufacturing cost. To this regard, scalable and high-throughput solution-processing fabrication techniques on large-area flexible substrates need to be optimized and established, aiming especially at fully printed or roll-to-roll manufacturing processes. \(^{37,87}\) Once these issues will be solved, flexible metal oxide semiconductor-based devices promise to be integrated into everyday objects, such as disposable and inexpensive consumer products like smart labels for food, water and plant monitoring, \(^{1,80,165}\) autonomous textile-integrated systems for healthcare, sport and automotive, \(^{5,6}\) conformable and stretchable devices for robotic artificial skins, \(^{19}\) as well as imperceptible and implantable prostheses or diagnostic tools. \(^{13,15,352}\) Even if at present there is still work to be done, the speed of development that this field has undergone in the last years let us foresee that flexible metal oxide semiconductor-based technology will play a key role in tomorrow’s electronic scenario.

**ACKNOWLEDGMENTS**

We acknowledge great input and fruitful discussions on the topic of flexible metal oxide semiconductor TFTs Dr. C. Zysset, Dr. T. Kinkeldei, Dr. G. A. Salvatore, A. Daus, S. Knobelspies (all ETH Zurich), Dr. K. Ishida, Dr. T. Meister, R. Shabanpour, Dr. B. Kheradmand-Boroujeni, Dr. C. Carta, Prof. Ellinger (all TU Dresden), Dr. P. Pattanasattayavong, Dr. Y-H. Lin, Dr. N. Yaacobi-Gross (all Imperial College), and Prof. S. Bauer (JKU Linz). This work was funded, in part, by the European Commission through the Seventh Framework Projects (FP7): Flexible multifunctional bendable integrated light-weight ultra-thin systems (FLEXIBILITY), grant agreement FP7-287568. This work was also partially funded by the SNF/DFG DACH FFlexCom project: Wireless Indium-Gallium-Zinc-Oxide Transmitters and Devices on Mechanically-Flexible Thin-Film Substrates (WISDOM), SNF grant number 160347.

**REFERENCES**


G. H. Gelinck, and B. Cobb, "Electroceramics, 1 (2015)."


M. Mativenga, D. Geng, B. Kim, and J. Jang, "Electroceramics, 1 (2015)."


S. M. Mativenga, D. Geng, B. Kim, and J. Jang, "Electroceramics, 1 (2015)."


S. M. Mativenga, D. Geng, B. Kim, and J. Jang, "Electroceramics, 1 (2015)."


360 J. Zhang, Y. Li, B. Zhang, H. Wang, Q. Xin, and A. Song, Nat. Commun. 6, 7561 (2015).